nRF24L01+

Single Chip 2.4GHz Transceiver

Product Specification v1.0

Key Features

- Worldwide 2.4GHz ISM band operation
- 250kbps, 1Mbps and 2Mbps on air data rates
- Ultra low power operation
- 11.3mA TX at 0dBm output power
- 13.5mA RX at 2Mbps air data rate
- 900nA in power down
- 26µA in standby-I
- On chip voltage regulator
- 1.9 to 3.6V supply range
- Enhanced ShockBurst™
- Automatic packet handling
- Auto packet transaction handling
- 6 data pipe MultiCeiver™
- Drop-in compatibility with nRF24L01
- On-air compatible in 250kbps and 1Mbps with nRF2401A, nRF2402, nRF24E1 and nRF24E2
- Low cost BOM
- ±60ppm 16MHz crystal
- 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

Applications

- Wireless PC Peripherals
- Mouse, keyboards and remotes
- 3-in-1 desktop bundles
- Advanced Media center remote controls
- VoIP headsets
- Game controllers
- Sports watches and sensors
- RF remote controls for consumer electronics
- Home and commercial automation
- Ultra low power sensor networks
- Active RFID
- Asset tracking systems
- Toys

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Objective product specification	This product specification contains target specifications for product development.
Preliminary product specification	This product specification contains preliminary data; supplementary data may be published from Nordic Semiconductor ASA later.
Product specification	This product specification contains final product specifications. Nordic Semiconductor ASA reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Contact details

Visit www.nordicsemi.no for Nordic Semiconductor sales offices and distributors worldwide

Main office:

Otto Nielsens vei 12
7004 Trondheim
Phone: +47 72 89 89 00
Fax: +47 72 89 89 89
www.nordicsemi.no

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Writing Conventions

This product specification follows a set of typographic rules that makes the document consistent and easy to read. The following writing conventions are used:

- Commands, bit state conditions, and register names are written in `Courier`.
- Pin names and pin signal conditions are written in **`Courier bold`**.
- Cross references are underlined and highlighted in blue.

Revision History

Date	Version	Description
September 2008	1.0	

Attention!

Observe precaution for handling
Electrostatic Sensitive Device.

HBM (Human Body Model) ≥ 1Kv
MM (Machine Model) ≥ 200V

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1 Introduction

The nRF24L01+ is a single chip 2.4GHz transceiver with an embedded baseband protocol engine (Enhanced ShockBurst™), suitable for ultra low power wireless applications. The nRF24L01+ is designed for operation in the world wide ISM frequency band at 2.400 - 2.4835GHz.

To design a radio system with the nRF24L01+, you simply need an MCU (microcontroller) and a few external passive components.

You can operate and configure the nRF24L01+ through a Serial Peripheral Interface (SPI). The register map, which is accessible through the SPI, contains all configuration registers in the nRF24L01+ and is accessible in all operation modes of the chip.

The embedded baseband protocol engine (Enhanced ShockBurst™) is based on packet communication and supports various modes from manual operation to advanced autonomous protocol operation. Internal FIFOs ensure a smooth data flow between the radio front end and the system's MCU. Enhanced ShockBurst™ reduces system cost by handling all the high speed link layer operations.

The radio front end uses GFSK modulation. It has user configurable parameters like frequency channel, output power and air data rate. nRF24L01+ supports an air data rate of 250 kbps, 1 Mbps and 2Mbps. The high air data rate combined with two power saving modes make the nRF24L01+ very suitable for ultra low power designs.

nRF24L01+ is drop-in compatible with nRF24L01 and on-air compatible with nRF2401A, nRF2402, nRF24E1 and nRF24E2. Intermodulation and wideband blocking values in nRF24L01+ are much improved in comparison to the nRF24L01 and the addition of internal filtering to nRF24L01+ has improved the margins for meeting RF regulatory standards.

Internal voltage regulators ensure a high Power Supply Rejection Ratio (PSRR) and a wide power supply range.

1.1 Features

Features of the nRF24L01+ include:

- Radio
  - Worldwide 2.4GHz ISM band operation
  - 126 RF channels
  - Common RX and TX interface
  - GFSK modulation
  - 250kbps, 1 and 2Mbps air data rate
  - 1MHz non-overlapping channel spacing at 1Mbps
  - 2MHz non-overlapping channel spacing at 2Mbps
- Transmitter
  - Programmable output power: 0, -6, -12 or -18dBm
  - 11.3mA at 0dBm output power
- Receiver
  - Fast AGC for improved dynamic range
  - Integrated channel filters
  - 13.5mA at 2Mbps
  - -82dBm sensitivity at 2Mbps
  - -85dBm sensitivity at 1Mbps
  - -94dBm sensitivity at 250kbps
- RF Synthesizer
  - Fully integrated synthesizer
  - No external loop filer, VCO varactor diode or resonator
  - Accepts low cost ±60ppm 16MHz crystal
- Enhanced ShockBurst™
  - 1 to 32 bytes dynamic payload length
  - Automatic packet handling
  - Auto packet transaction handling
  - 6 data pipe MultiCeiver™ for 1:6 star networks
- Power Management
  - Integrated voltage regulator
  - 1.9 to 3.6V supply range
  - Idle modes with fast start-up times for advanced power management
  - 26µA Standby-I mode, 900nA power down mode
  - Max 1.5ms start-up from power down mode
  - Max 130us start-up from standby-I mode
- Host Interface
  - 4-pin hardware SPI
  - Max 10Mbps
  - 3 separate 32 bytes TX and RX FIFOs
  - 5V tolerant inputs
- Compact 20-pin 4x4mm QFN package

1.2 Block diagram

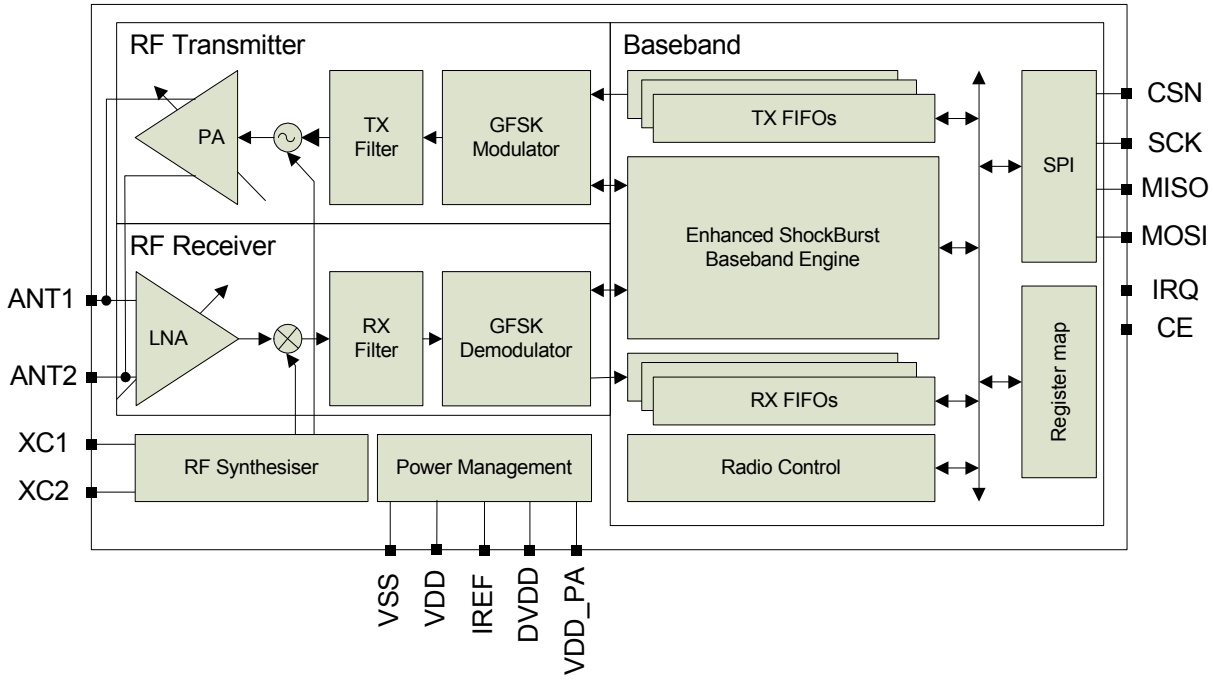


Figure 1. nRF24L01+ block diagram

2 Pin Information

2.1 Pin assignment

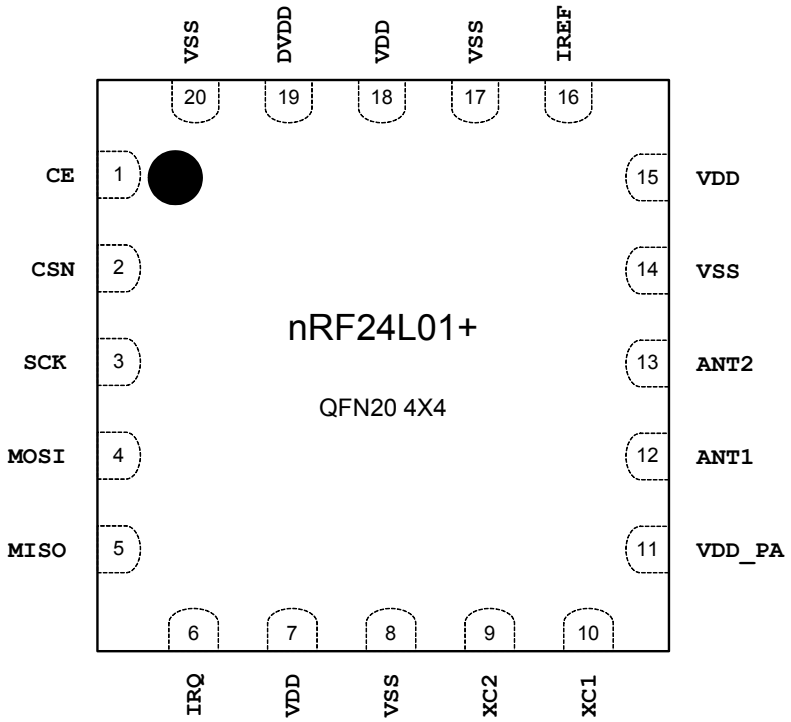


Figure 2. nRF24L01+ pin assignment (top view) for the QFN20 4x4 package

2.2 Pin functions

Pin	Name	Pin function	Description
1	CE	Digital Input	Chip Enable Activates RX or TX mode
2	CSN	Digital Input	SPI Chip Select
3	SCK	Digital Input	SPI Clock
4	MOSI	Digital Input	SPI Slave Data Input
5	MISO	Digital Output	SPI Slave Data Output, with tri-state option
6	IRQ	Digital Output	Maskable interrupt pin. Active low
7	VDD	Power	Power Supply (+1.9V - +3.6V DC)
8	VSS	Power	Ground (0V)
9	XC2	Analog Output	Crystal Pin 2
10	XC1	Analog Input	Crystal Pin 1
11	VDD_PA	Power Output	Power Supply Output (+1.8V) for the internal nRF24L01+ Power Amplifier. Must be connected to ANT1 and ANT2 as shown in Figure 32.
12	ANT1	RF	Antenna interface 1
13	ANT2	RF	Antenna interface 2
14	VSS	Power	Ground (0V)
15	VDD	Power	Power Supply (+1.9V - +3.6V DC)
16	IREF	Analog Input	Reference current. Connect a 22kΩ resistor to ground. See Figure 32.
17	VSS	Power	Ground (0V)
18	VDD	Power	Power Supply (+1.9V - +3.6V DC)
19	DVDD	Power Output	Internal digital supply output for de-coupling purposes. See Figure 32.
20	VSS	Power	Ground (0V)

Table 1. nRF24L01+ pin function

3 Absolute maximum ratings

Note: Exceeding one or more of the limiting values may cause permanent damage to nRF24L01+.

Operating conditions	Minimum	Maximum	Units
Supply voltages			
VDD	-0.3	3.6	V
VSS		0	V
Input voltage			
V_I	-0.3	5.25	V
Output voltage			
V_O	VSS to VDD	VSS to VDD	
Total Power Dissipation			
P_D (T_A=85°C)		60	mW
Temperatures			
Operating Temperature	-40	+85	°C
Storage Temperature	-40	+125	°C

Table 2. Absolute maximum ratings

4 Operating conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
VDD	Supply voltage		1.9	3.0	3.6	V
VDD	Supply voltage if input signals >3.6V		2.7	3.0	3.3	V
TEMP	Operating Temperature		-40	+27	+85	ºC

Table 3. Operating conditions

5 Electrical specifications

Conditions: VDD = +3V, VSS = 0V, T_A = - 40ºC to + 85ºC

5.1 Power consumption

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	Idle modes					
I_{VDD_PD}	Supply current in power down			900		nA
I_{VDD_ST1}	Supply current in standby-I mode	a		26		µA
I_{VDD_ST2}	Supply current in standby-II mode			320		µA
I_{VDD_SU}	Average current during 1.5ms crystal oscillator startup			400		µA
	Transmit					
I_{VDD_TX0}	Supply current @ 0dBm output power	b		11.3		mA
I_{VDD_TX6}	Supply current @ -6dBm output power	b		9.0		mA
I_{VDD_TX12}	Supply current @ -12dBm output power	b		7.5		mA
I_{VDD_TX18}	Supply current @ -18dBm output power	b		7.0		mA
I_{VDD_AVG}	Average Supply current @ -6dBm output power, ShockBurst™	c		0.12		mA
I_{VDD_TXS}	Average current during TX settling	d		8.0		mA
	Receive					
I_{VDD_2M}	Supply current 2Mbps			13.5		mA
I_{VDD_1M}	Supply current 1Mbps			13.1		mA
I_{VDD_250}	Supply current 250kbps			12.6		mA
I_{VDD_RXS}	Average current during RX settling	e		8.9		mA

a. This current is for a 12pF crystal. Current when using external clock is dependent on signal swing.
b. Antenna load impedance = 15Ω+j88Ω..
c. Antenna load impedance = 15Ω+j88Ω. Average data rate 10kbps and max. payload length packets.
d. Average current consumption during TX startup (130µs) and when changing mode from RX to TX (130µs).
e. Average current consumption during RX startup (130µs) and when changing mode from TX to RX (130µs).

Table 4. Power consumption

5.2 General RF conditions

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
f_{OP}	Operating frequency	a	2400		2525	MHz
PLL_{res}	PLL Programming resolution			1		MHz
f_{XTAL}	Crystal frequency			16		MHz
Δf_{250}	Frequency deviation @ 250kbps			±160		kHz
Δf_{1M}	Frequency deviation @ 1Mbps			±160		kHz
Δf_{2M}	Frequency deviation @ 2Mbps			±320		kHz
R_{GFSK}	Air Data rate	b	250		2000	kbps
$F_{CHANNEL\ 1M}$	Non-overlapping channel spacing @ 250kbps/ 1Mbps	c		1		MHz
$F_{CHANNEL\ 2M}$	Non-overlapping channel spacing @ 2Mbps	c		2		MHz

a. Regulatory standards determine the band range you can use.
b. Data rate in each burst on-air
c. The minimum channel spacing is 1MHz

Table 5. General RF conditions

5.3 Transmitter operation

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
P_{RF}	Maximum Output Power	a		0	+4	dBm
P_{RFC}	RF Power Control Range		16	18	20	dB
P_{RFCR}	RF Power Accuracy				±4	dB
P_{BW2}	20dB Bandwidth for Modulated Carrier (2Mbps)			1800	2000	kHz
P_{BW1}	20dB Bandwidth for Modulated Carrier (1Mbps)			900	1000	kHz
P_{BW250}	20dB Bandwidth for Modulated Carrier (250kbps)			700	800	kHz
$P_{RF1.2}$	1^{st} Adjacent Channel Transmit Power 2MHz (2Mbps)				-20	dBc
$P_{RF2.2}$	2^{nd} Adjacent Channel Transmit Power 4MHz (2Mbps)				-50	dBc
$P_{RF1.1}$	1^{st} Adjacent Channel Transmit Power 1MHz (1Mbps)				-20	dBc
$P_{RF2.1}$	2^{nd} Adjacent Channel Transmit Power 2MHz (1Mbps)				-45	dBc
$P_{RF1.250}$	1^{st} Adjacent Channel Transmit Power 1MHz (250kbps)				-30	dBc
$P_{RF2.250}$	2^{nd} Adjacent Channel Transmit Power 2MHz (250kbps)				-45	dBc

a. Antenna load impedance = 15Ω+j88Ω

Table 6. Transmitter operation

5.4 Receiver operation

Datarate	Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
	RX_{max}	Maximum received signal at <0.1% BER			0		dBm
2Mbps	RX_{SENS}	Sensitivity (0.1%BER) @2Mbps			-82		dBm
1Mbps	RX_{SENS}	Sensitivity (0.1%BER) @1Mbps			-85		dBm
250kbps	RX_{SENS}	Sensitivity (0.1%BER) @250kbps			-94		dBm

Table 7. RX Sensitivity

Datarate	Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
2Mbps	C/I_{CO}	C/I Co-channel			7		dBc
	C/I_{1ST}	1^{st} ACS (Adjacent Channel Selectivity) C/I 2MHz			3		dBc
	C/I_{2ND}	2^{nd} ACS C/I 4MHz			-17		dBc
	C/I_{3RD}	3^{rd} ACS C/I 6MHz			-21		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 12MHz			-40		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 36MHz	a		-48		dBc
1Mbps	C/I_{CO}	C/I Co-channel			9		dBc
	C/I_{1ST}	1^{st} ACS C/I 1MHz			8		dBc
	C/I_{2ND}	2^{nd} ACS C/I 2MHz			-20		dBc
	C/I_{3RD}	3^{rd} ACS C/I 3MHz			-30		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 6MHz			-40		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 25MHz	a		-47		dBc
250kbps	C/I_{CO}	C/I Co-channel			12		dBc
	C/I_{1ST}	1^{st} ACS C/I 1MHz			-12		dBc
	C/I_{2ND}	2^{nd} ACS C/I 2MHz			-33		dBc
	C/I_{3RD}	3^{rd} ACS C/I 3MHz			-38		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 6MHz			-50		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 25MHz	a		-60		dBc

a. **Narrow Band (In Band) Blocking measurements:**
0 to ±40MHz; 1MHz step size
For Interferer frequency offsets n*2*fxtal, blocking performance is degraded by approximately 5dB compared to adjacent figures.

Table 8. RX selectivity according to ETSI EN 300 440-1 V1.3.1 (2001-09) page 27

Datarate	Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
2Mbps	C/I_{CO}	C/I Co-channel (Modulated carrier)			11		dBc
	C/I_{1ST}	1^{st} ACS C/I 2MHz			4		dBc
	C/I_{2ND}	2^{nd} ACS C/I 4MHz			-18		dBc
	C/I_{3RD}	3^{rd} ACS C/I 6MHz			-24		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 12MHz			-40		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 36MHz	a		-48		dBc
1Mbps	C/I_{CO}	C/I Co-channel			12		dBc
	C/I_{1ST}	1^{st} ACS C/I 1MHz			8		dBc
	C/I_{2ND}	2^{nd} ACS C/I 2MHz			-21		dBc
	C/I_{3RD}	3^{rd} ACS C/I 3MHz			-30		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 6MHz			-40		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i > 25MHz	a		-50		dBc
250kbps	C/I_{CO}	C/I Co-channel			7		dBc
	C/I_{1ST}	1^{st} ACS C/I 1MHz			-12		dBc
	C/I_{2ND}	2^{nd} ACS C/I 2MHz			-34		dBc
	C/I_{3RD}	3^{rd} ACS C/I 3MHz			-39		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i >6MHz			-50		dBc
	C/I_{Nth}	N^{th} ACS C/I, f_i >25MHz	a		-60		dBc

a. **Narrow Band (In Band) Blocking measurements:**
0 to ±40MHz; 1MHz step size
Wide Band Blocking measurements:
30MHz to 2000MHz; 10MHz step size
2000MHz to 2399MHz; 3MHz step size
2484MHz to 3000MHz; 3MHz step size
3GHz to 12.75GHz; 25MHz step size
Wanted signal for wideband blocking measurements:
-67dBm in 1Mbps and 2Mbps mode
-77dBm in 250kbps mode
For Interferer frequency offsets n*2*fxtal, blocking performance are degraded by approximately 5dB compared to adjacent figures.
If the wanted signal is 3dB or more above the sensitivity level then, the carrier/interferer ratio is independent of the wanted signal level for a given frequency offset.

Table 9. RX selectivity with nRF24L01+ equal modulation on interfering signal. Measured using Pin = -67dBm for wanted signal.

Datarate	Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
2Mbps	P_IM(6	Input power of IM interferers at 6 and 12MHz offset from wanted signal			-42		dBm
	P_IM(8)	Input power of IM interferers at 8 and 16MHz offset from wanted signal			-38		dBm
	P_IM(10)	Input power of IM interferers at 10 and 20MHz offset from wanted signal			-37		dBm
1Mbps	P_IM(3)	Input power of IM interferers at 3 and 6MHz offset from wanted signal			-36		dBm
	P_IM(4)	Input power of IM interferers at 4 and 8MHz offset from wanted signal			-36		dBm
	P_IM(5)	Input power of IM interferers at 5 and 10MHz offset from wanted signal			-36		dBm
250kbps	P_IM(3)	Input power of IM interferers at 3 and 6MHz offset from wanted signal			-36		dBm
	P_IM(4)	Input power of IM interferers at 4 and 8MHz offset from wanted signal			-36		dBm
	P_IM(5)	Input power of IM interferers at 5 and 10MHz offset from wanted signal			-36		dBm

Note: Wanted signal level at Pin = -64 dBm. Two interferers with equal input power are used. The interferer closest in frequency is unmodulated, the other interferer is modulated equal with the wanted signal. The input power of interferers where the sensitivity equals BER = 0.1% is presented.

Table 10. RX intermodulation test performed according to Bluetooth Specification version 2.0

5.5 Crystal specifications

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
Fxo	Crystal Frequency			16		MHz
ΔF	Tolerance	a b			±60	ppm
C_0	Equivalent parallel capacitance			1.5	7.0	pF
Ls	Equivalent serial inductance	c		30		mH
C_L	Load capacitance		8	12	16	pF
ESR	Equivalent Series Resistance				100	Ω

a. Frequency accuracy including; tolerance at 25°C, temperature drift, aging and crystal loading.
b. Frequency regulations in certain regions set tighter requirements for frequency tolerance (For example, Japan and South Korea specify max. +/- 50ppm).
c. Startup time from power down to standby mode is dependant on the Ls parameter. See Table 16. on page 24 for details.

Table 11. Crystal specifications

The crystal oscillator startup time is proportional to the crystal equivalent inductance. The trend in crystal design is to reduce the physical outline. An effect of a small outline is an increase in equivalent serial inductance Ls, which gives a longer startup time. The maximum crystal oscillator startup time, Tpd2stby = 1.5 ms, is set using a crystal with equivalent serial inductance of maximum 30mH.

An application specific worst case startup time can be calculated as :

Tpd2stby= Ls/30mH *1.5ms if Ls exceeds 30mH.

Note: In some crystal datasheets Ls is called L1 or Lm and Cs is called C1 or Cm.

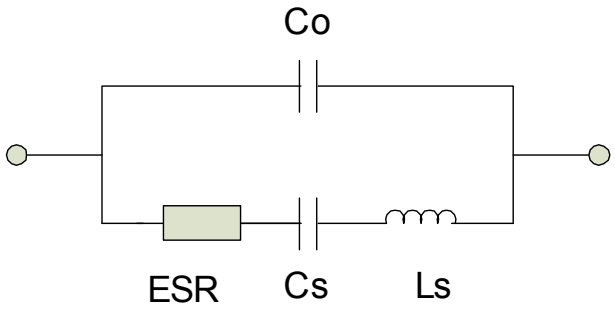


Figure 3. Equivalent crystal components

5.6 DC characteristics

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{IH}	HIGH level input voltage		0.7VDD		5.25[a]	V
V_{IL}	LOW level input voltage		VSS		0.3VDD	V

a. If the input signal >3.6V, the VDD of the nRF24L01+ must be between 2.7V and 3.3V (3.0V±10%)

Table 12. Digital input pin

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
V_{OH}	HIGH level output voltage (I_{OH}=-0.25mA)		VDD -0.3		VDD	V
V_{OL}	LOW level output voltage (I_{OL}=0.25mA)				0.3	V

Table 13. Digital output pin

5.7 Power on reset

Symbol	Parameter (condition)	Notes	Min.	Typ.	Max.	Units
T_{PUP}	Power ramp up time	a			100	ms
T_{POR}	Power on reset	b	1		100	ms

a. From 0V to 1.9V.
b. Measured from when the VDD reaches 1.9V to when the reset finishes.

Table 14. Power on reset

6 Radio Control

This chapter describes the nRF24L01+ radio transceiver's operating modes and the parameters used to control the radio.

The nRF24L01+ has a built-in state machine that controls the transitions between the chip's operating modes. The state machine takes input from user defined register values and internal signals.

6.1 Operational Modes

You can configure the nRF24L01+ in power down, standby, RX or TX mode. This section describes these modes in detail.

6.1.1 State diagram

The state diagram in Figure 4. shows the operating modes and how they function. There are three types of distinct states highlighted in the state diagram:

- **Recommended operating mode:** is a recommended state used during normal operation.
- **Possible operating mode:** is a possible operating state, but is not used during normal operation.
- **Transition state:** is a time limited state used during start up of the oscillator and settling of the PLL.

When the VDD reaches 1.9V or higher nRF24L01+ enters the Power on reset state where it remains in reset until entering the Power Down mode.

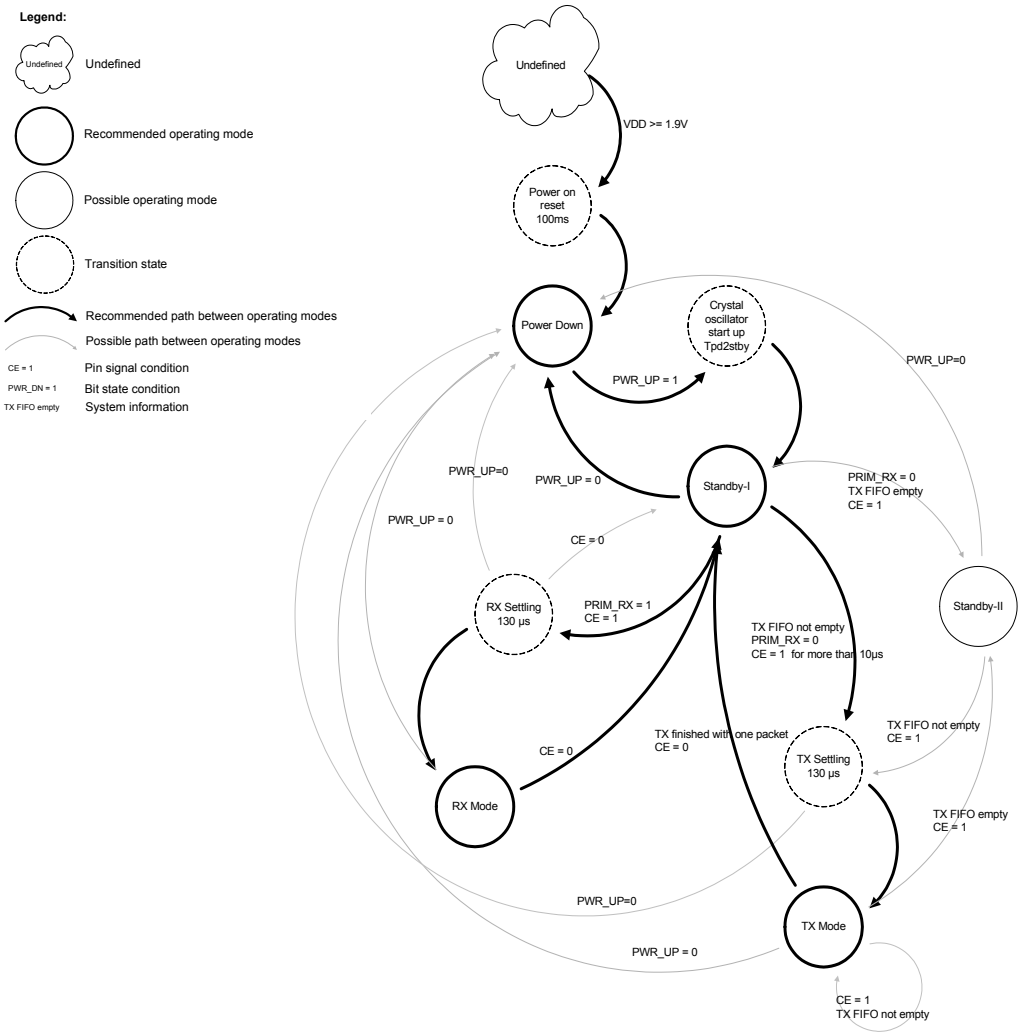


Figure 4. Radio control state diagram

6.1.2 Power Down Mode

In power down mode nRF24L01+ is disabled using minimal current consumption. All register values available are maintained and the SPI is kept active, enabling change of configuration and the uploading/downloading of data registers. For start up times see Table 16. on page 24. Power down mode is entered by setting the PWR_UP bit in the CONFIG register low.

6.1.3 Standby Modes

6.1.3.1 Standby-I mode

By setting the PWR_UP bit in the CONFIG register to 1, the device enters standby-I mode. Standby-I mode is used to minimize average current consumption while maintaining short start up times. In this mode only part of the crystal oscillator is active. Change to active modes only happens if **CE** is set high and when **CE** is set low, the nRF24L01 returns to standby-I mode from both the TX and RX modes.

6.1.3.2 Standby-II mode

In standby-II mode extra clock buffers are active and more current is used compared to standby-I mode. nRF24L01+ enters standby-II mode if **CE** is held high on a PTX device with an empty TX FIFO. If a new packet is uploaded to the TX FIFO, the PLL immediately starts and the packet is transmitted after the normal PLL settling delay (130µs).

Register values are maintained and the SPI can be activated during both standby modes. For start up times see Table 16. on page 24.

6.1.4 RX mode

The RX mode is an active mode where the nRF24L01+ radio is used as a receiver. To enter this mode, the nRF24L01+ must have the `PWR_UP` bit, `PRIM_RX` bit and the **CE** pin set high.

In RX mode the receiver demodulates the signals from the RF channel, constantly presenting the demodulated data to the baseband protocol engine. The baseband protocol engine constantly searches for a valid packet. If a valid packet is found (by a matching address and a valid CRC) the payload of the packet is presented in a vacant slot in the RX FIFOs. If the RX FIFOs are full, the received packet is discarded.

The nRF24L01+ remains in RX mode until the MCU configures it to standby-I mode or power down mode. However, if the automatic protocol features (Enhanced ShockBurst™) in the baseband protocol engine are enabled, the nRF24L01+ can enter other modes in order to execute the protocol.

In RX mode a Received Power Detector (RPD) signal is available. The RPD is a signal that is set high when a RF signal higher than -64 dBm is detected inside the receiving frequency channel. The internal `RPD` signal is filtered before presented to the `RPD` register. The RF signal must be present for at least 40µs before the `RPD` is set high. How to use the RPD is described in Section 6.4 on page 25.

6.1.5 TX mode

The TX mode is an active mode for transmitting packets. To enter this mode, the nRF24L01+ must have the `PWR_UP` bit set high, `PRIM_RX` bit set low, a payload in the TX FIFO and a high pulse on the **CE** for more than 10µs.

The nRF24L01+ stays in TX mode until it finishes transmitting a packet. If **CE** = 0, nRF24L01+ returns to standby-I mode. If **CE** = 1, the status of the TX FIFO determines the next action. If the TX FIFO is not empty the nRF24L01+ remains in TX mode and transmits the next packet. If the TX FIFO is empty the nRF24L01+ goes into standby-II mode. The nRF24L01+ transmitter PLL operates in open loop when in TX mode. It is important never to keep the nRF24L01+ in TX mode for more than 4ms at a time. If the Enhanced ShockBurst™ features are enabled, nRF24L01+ is never in TX mode longer than 4ms.

6.1.6 Operational modes configuration

The following table (Table 15.) describes how to configure the operational modes.

Mode	PWR_UP register	PRIM_RX register	CE input pin	FIFO state
RX mode	1	1	1	-
TX mode	1	0	1	Data in TX FIFOs. Will empty all levels in TX FIFOs[a].
TX mode	1	0	Minimum 10µs high pulse	Data in TX FIFOs.Will empty one level in TX FIFOs[b].
Standby-II	1	0	1	TX FIFO empty.
Standby-I	1	-	0	No ongoing packet transmission.
Power Down	0	-	-	-

a. If **CE** is held high all TX FIFOs are emptied and all necessary ACK and possible retransmits are carried out. The transmission continues as long as the TX FIFO is refilled. If the TX FIFO is empty when the **CE** is still high, nRF24L01+ enters standby-II mode. In this mode the transmission of a packet is started as soon as the **CSN** is set high after an upload (UL) of a packet to TX FIFO.

b. This operating mode pulses the **CE** high for at least 10µs. This allows one packet to be transmitted. This is the normal operating mode. After the packet is transmitted, the nRF24L01+ enters standby-I mode.

Table 15. nRF24L01+ main modes

6.1.7 Timing Information

The timing information in this section relates to the transitions between modes and the timing for the **CE** pin. The transition from TX mode to RX mode or vice versa is the same as the transition from the standby modes to TX mode or RX mode (max. 130µs), as described in Table 16.

Name	nRF24L01+	Notes	Max.	Min.	Comments
Tpd2stby	Power Down ➔ Standby mode		150µs		With external clock
		a	1.5ms		External crystal, Ls < 30mH
			3ms		External crystal, Ls = 60mH
			4.5ms		External crystal, Ls = 90mH
Tstby2a	Standby modes ➔ TX/RX mode		130µs		
Thce	Minimum **CE** high			10µs	
Tpece2csn	Delay from **CE** positive edge to **CSN** low			4µs	

a. See Table 11. on page 19 for crystal specifications.

Table 16. Operational timing of nRF24L01+

For nRF24L01+ to go from power down mode to TX or RX mode it must first pass through stand-by mode. There must be a delay of Tpd2stby (see Table 16.) after the nRF24L01+ leaves power down mode before the **CE** is set high.

Note: If **VDD** is turned off the register value is lost and you must configure nRF24L01+ before entering the TX or RX modes.

6.2 Air data rate

The air data rate is the modulated signaling rate the nRF24L01+ uses when transmitting and receiving data. It can be 250kbps, 1Mbps or 2Mbps. Using lower air data rate gives better receiver sensitivity than higher air data rate. But, high air data rate gives lower average current consumption and reduced probability of on-air collisions.

The air data rate is set by the `RF_DR` bit in the `RF_SETUP` register. A transmitter and a receiver must be programmed with the same air data rate to communicate with each other.

nRF24L01+ is fully compatible with nRF24L01. For compatibility with nRF2401A, nRF2402, nRF24E1, and nRF24E2 the air data rate must be set to 250kbps or 1Mbps.

6.3 RF channel frequency

The RF channel frequency determines the center of the channel used by the nRF24L01+. The channel occupies a bandwidth of less than 1MHz at 250kbps and 1Mbps and a bandwidth of less than 2MHz at 2Mbps. nRF24L01+ can operate on frequencies from 2.400GHz to 2.525GHz. The programming resolution of the RF channel frequency setting is 1MHz.

At 2Mbps the channel occupies a bandwidth wider than the resolution of the RF channel frequency setting. To ensure non-overlapping channels in 2Mbps mode, the channel spacing must be 2MHz or more. At 1Mbps and 250kbps the channel bandwidth is the same or lower than the resolution of the RF frequency.

The RF channel frequency is set by the `RF_CH` register according to the following formula:

$F_0 = 2400 + RF_CH$ *[MHz]*

You must program a transmitter and a receiver with the same RF channel frequency to communicate with each other.

6.4 Received Power Detector measurements

Received Power Detector (RPD), located in register 09, bit 0, triggers at received power levels above -64 dBm that are present in the RF channel you receive on. If the received power is less than -64 dBm, RDP = 0.

The RPD can be read out at any time while nRF24L01+ is in receive mode. This offers a snapshot of the current received power level in the channel. The RPD status is latched when a valid packet is received which then indicates signal strength from your own transmitter. If no packets are received the RPD is latched at the end of a receive period as a result of host MCU setting CE low or RX time out controlled by Enhanced ShockBurst™.

The status of RPD is correct when RX mode is enabled and after a wait time of Tstby2a +Tdelay_AGC= 130us + 40us. The RX gain varies over temperature which means that the RPD threshold also varies over temperature. The RPD threshold value is reduced by - 5dB at T = -40°C and increased by + 5dB at 85°C.

6.5 PA control

The PA (Power Amplifier) control is used to set the output power from the nRF24L01+ power amplifier. In TX mode PA control has four programmable steps, see Table 17.

The PA control is set by the RF_PWR bits in the RF_SETUP register.

SPI RF-SETUP (RF_PWR)	RF output power	DC current consumption
11	0dBm	11.3mA
10	-6dBm	9.0mA
01	-12dBm	7.5mA
00	-18dBm	7.0mA

Conditions: VDD = 3.0V, VSS = 0V, T_A = 27ºC, Load impedance = 15Ω+j88Ω.

Table 17. RF output power setting for the nRF24L01+

6.6 RX/TX control

The RX/TX control is set by PRIM_RX bit in the CONFIG register and sets the nRF24L01+ in transmit/ receive mode.

7 Enhanced ShockBurst™

Enhanced ShockBurst™ is a packet based data link layer that features automatic packet assembly and timing, automatic acknowledgement and retransmissions of packets. Enhanced ShockBurst™ enables the implementation of ultra low power and high performance communication with low cost host microcontrollers. The Enhanced ShockBurst™ features enable significant improvements of power efficiency for bi-directional and uni-directional systems, without adding complexity on the host controller side.

7.1 Features

The main features of Enhanced ShockBurst™ are:

- 1 to 32 bytes dynamic payload length
- Automatic packet handling
- Automatic packet transaction handling
  - Auto Acknowledgement with payload
  - Auto retransmit
- 6 data pipe MultiCeiver™ for 1:6 star networks

7.2 Enhanced ShockBurst™ overview

Enhanced ShockBurst™ uses ShockBurst™ for automatic packet handling and timing. During transmit, ShockBurst™ assembles the packet and clocks the bits in the data packet for transmission. During receive, ShockBurst™ constantly searches for a valid address in the demodulated signal. When ShockBurst™ finds a valid address, it processes the rest of the packet and validates it by CRC. If the packet is valid the payload is moved into a vacant slot in the RX FIFOs. All high speed bit handling and timing is controlled by ShockBurst™.

Enhanced ShockBurst™ features automatic packet transaction handling for the easy implementation of a reliable bi-directional data link. An Enhanced ShockBurst™ packet transaction is a packet exchange between two transceivers, with one transceiver acting as the Primary Receiver (PRX) and the other transceiver acting as the Primary Transmitter (PTX). An Enhanced ShockBurst™ packet transaction is always initiated by a packet transmission from the PTX, the transaction is complete when the PTX has received an acknowledgment packet (ACK packet) from the PRX. The PRX can attach user data to the ACK packet enabling a bi-directional data link.

The automatic packet transaction handling works as follows:

1. You begin the transaction by transmitting a data packet from the PTX to the PRX. Enhanced ShockBurst™ automatically sets the PTX in receive mode to wait for the ACK packet.
2. If the packet is received by the PRX, Enhanced ShockBurst™ automatically assembles and transmits an acknowledgment packet (ACK packet) to the PTX before returning to receive mode.
3. If the PTX does not receive the ACK packet immediately, Enhanced ShockBurst™ automatically retransmits the original data packet after a programmable delay and sets the PTX in receive mode to wait for the ACK packet.

In Enhanced ShockBurst™ it is possible to configure parameters such as the maximum number of retransmits and the delay from one transmission to the next retransmission. All automatic handling is done without the involvement of the MCU.

7.3 Enhanced Shockburst™ packet format

The format of the Enhanced ShockBurst™ packet is described in this section. The Enhanced Shock-Burst™ packet contains a preamble, address, packet control, payload and CRC field. Figure 5. shows the packet format with MSB to the left.

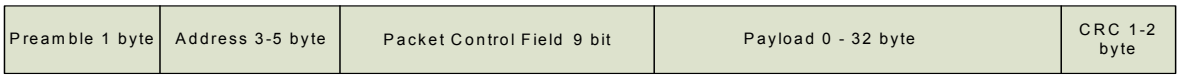


Figure 5. An Enhanced ShockBurst™ packet with payload (0-32 bytes)

7.3.1 Preamble

The preamble is a bit sequence used to synchronize the receivers demodulator to the incoming bit stream. The preamble is one byte long and is either 01010101 or 10101010. If the first bit in the address is 1 the preamble is automatically set to 10101010 and if the first bit is 0 the preamble is automatically set to 01010101. This is done to ensure there are enough transitions in the preamble to stabilize the receiver.

7.3.2 Address

This is the address for the receiver. An address ensures that the packet is detected and received by the correct receiver, preventing accidental cross talk between multiple nRF24L01+ systems. You can configure the address field width in the `AW` register to be 3, 4 or 5 bytes, see Table 28. on page 63.

Note: Addresses where the level shifts only one time (that is, 000FFFFFFF) can often be detected in noise and can give a false detection, which may give a raised Packet Error Rate. Addresses as a continuation of the preamble (hi-low toggling) also raises the Packet Error Rate.

7.3.3 Packet control field

Figure 6. shows the format of the 9 bit packet control field, MSB to the left.

Figure 6. Packet control field

The packet control field contains a 6 bit payload length field, a 2 bit PID (Packet Identity) field and a 1 bit `NO_ACK` flag.

7.3.3.1 Payload length

This 6 bit field specifies the length of the payload in bytes. The length of the payload can be from 0 to 32 bytes.

Coding: 000000 = 0 byte (only used in empty ACK packets.) 100000 = 32 byte, 100001 = Don't care.

This field is only used if the Dynamic Payload Length function is enabled.

7.3.3.2 PID (Packet identification)

The 2 bit PID field is used to detect if the received packet is new or retransmitted. PID prevents the PRX device from presenting the same payload more than once to the receiving host MCU. The PID field is incremented at the TX side for each new packet received through the SPI. The PID and CRC fields (see section 7.3.5 on page 30) are used by the PRX device to determine if a packet is retransmitted or new. When several data packets are lost on the link, the PID fields may become equal to the last received PID. If a packet has the same PID as the previous packet, nRF24L01+ compares the CRC sums from both packets. If the CRC sums are also equal, the last received packet is considered a copy of the previously received packet and discarded.

7.3.3.3 No Acknowledgment flag (NO_ACK)

The Selective Auto Acknowledgement feature controls the NO_ACK flag.

This flag is only used when the auto acknowledgement feature is used. Setting the flag high tells the receiver that the packet is not to be auto acknowledged.

On the PTX you can set the NO_ACK flag bit in the Packet Control Field with this command:

W_TX_PAYLOAD_NOACK

However, the function must first be enabled in the FEATURE register by setting the EN_DYN_ACK bit. When you use this option the PTX goes directly to standby-I mode after transmitting the packet. The PRX does not transmit an ACK packet when it receives the packet.

7.3.4 Payload

The payload is the user defined content of the packet. It can be 0 to 32 bytes wide and is transmitted on-air when it is uploaded to nRF24L01+.

Enhanced ShockBurst™ provides two alternatives for handling payload lengths; static and dynamic.

The default is static payload length. With static payload length all packets between a transmitter and a receiver have the same length. Static payload length is set by the RX_PW_Px registers on the receiver side. The payload length on the transmitter side is set by the number of bytes clocked into the TX_FIFO and must equal the value in the RX_PW_Px register on the receiver side.

Dynamic Payload Length (DPL) is an alternative to static payload length. DPL enables the transmitter to send packets with variable payload length to the receiver. This means that for a system with different payload lengths it is not necessary to scale the packet length to the longest payload.

With the DPL feature the nRF24L01+ can decode the payload length of the received packet automatically instead of using the RX_PW_Px registers. The MCU can read the length of the received payload by using the R_RX_PL_WID command.

Note: Always check if the packet width reported is 32 bytes or shorter when using the R_RX_PL_WID command. If its width is longer than 32 bytes then the packet contains errors and must be discarded. Discard the packet by using the Flush_RX command.

In order to enable DPL the EN_DPL bit in the FEATURE register must be enabled. In RX mode the DYNPD register must be set. A PTX that transmits to a PRX with DPL enabled must have the DPL_P0 bit in DYNPD set.

7.3.5 CRC (Cyclic Redundancy Check)

The CRC is the mandatory error detection mechanism in the packet. It is either 1 or 2 bytes and is calculated over the address, Packet Control Field and Payload.

The polynomial for 1 byte CRC is $X^8 + X^2 + X + 1$. Initial value 0xFF.

The polynomial for 2 byte CRC is $X^{16} + X^{12} + X^5 + 1$. Initial value 0xFFFF.

The number of bytes in the CRC is set by the CRCO bit in the CONFIG register. No packet is accepted by Enhanced ShockBurst™ if the CRC fails.

7.3.6 Automatic packet assembly

The automatic packet assembly assembles the preamble, address, packet control field, payload and CRC to make a complete packet before it is transmitted.

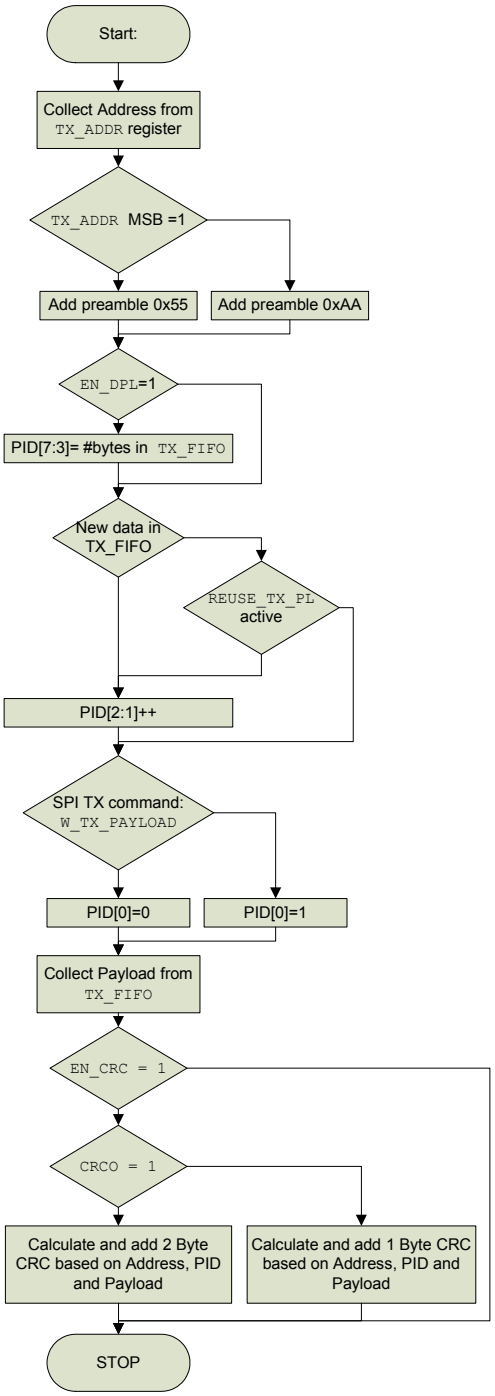


Figure 7. Automatic packet assembly

7.3.7 Automatic packet disassembly

After the packet is validated, Enhanced ShockBurst™ disassembles the packet and loads the payload into the RX FIFO, and asserts the RX_DR IRQ.

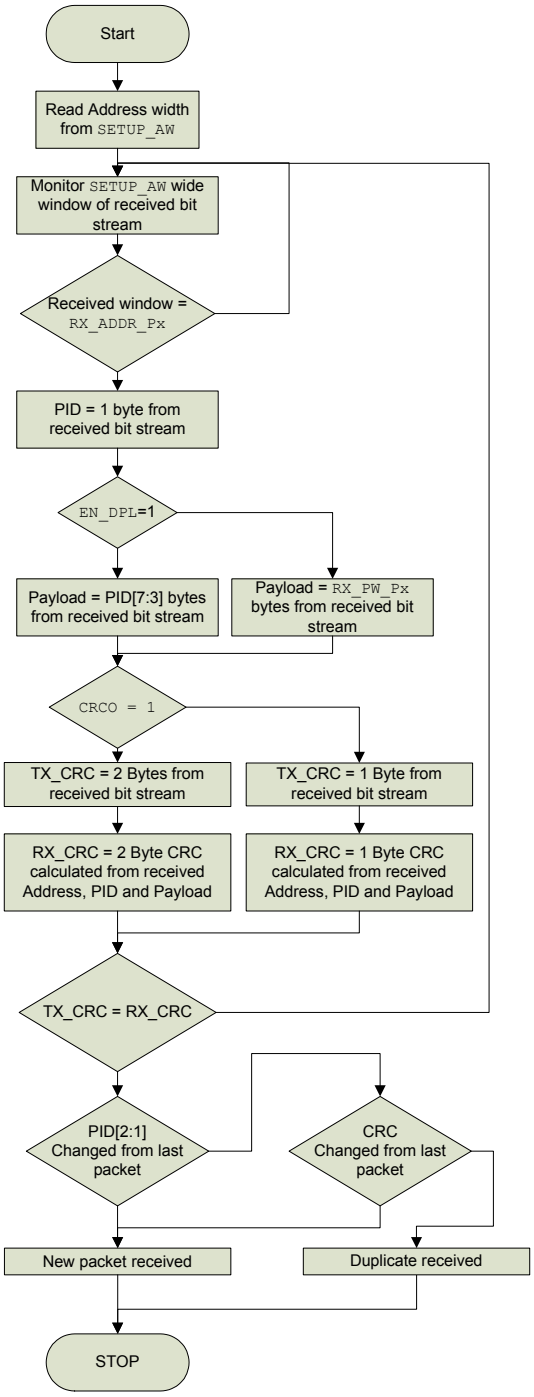


Figure 8. Automatic packet disassembly

7.4 Automatic packet transaction handling

Enhanced ShockBurst™ has two functions for automatic packet transaction handling; auto acknowledgement and auto re-transmit.

7.4.1 Auto acknowledgement

Auto acknowledgment is a function that automatically transmits an ACK packet to the PTX after it has received and validated a packet. The auto acknowledgement function reduces the load of the system MCU and can remove the need for dedicated SPI hardware. This also reduces cost and average current consumption. The Auto Acknowledgement feature is enabled by setting the `EN_AA` register.

Note: If the received packet has the `NO_ACK` flag set, auto acknowledgement is not executed.

An ACK packet can contain an optional payload from PRX to PTX. In order to use this feature, the Dynamic Payload Length (DPL) feature must be enabled. The MCU on the PRX side has to upload the payload by clocking it into the TX FIFO by using the `W_ACK_PAYLOAD` command. The payload is pending in the TX FIFO (PRX) until a new packet is received from the PTX. nRF24L01+ can have three ACK packet payloads pending in the TX FIFO (PRX) at the same time.

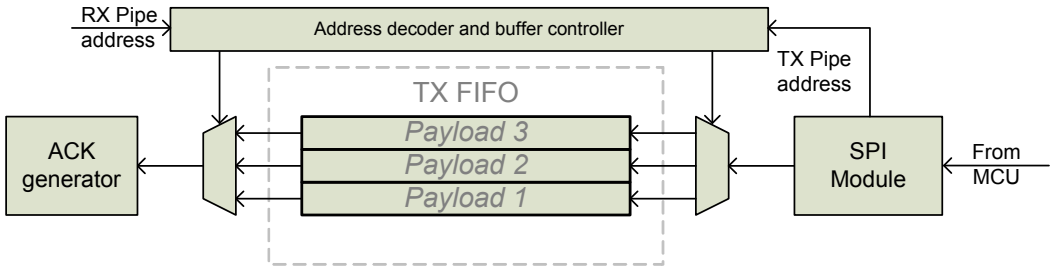


Figure 9. TX FIFO (PRX) with pending payloads

Figure 9. shows how the TX FIFO (PRX) is operated when handling pending ACK packet payloads. From the MCU the payload is clocked in with the `W_ACK_PAYLOAD` command. The address decoder and buffer controller ensure that the payload is stored in a vacant slot in the TX FIFO (PRX). When a packet is received, the address decoder and buffer controller are notified with the PTX address. This ensures that the right payload is presented to the ACK generator.

If the TX FIFO (PRX) contains more than one payload to a PTX, payloads are handled using the first in – first out principle. The TX FIFO (PRX) is blocked if all pending payloads are addressed to a PTX where the link is lost. In this case, the MCU can flush the TX FIFO (PRX) by using the `FLUSH_TX` command.

In order to enable Auto Acknowledgement with payload the `EN_ACK_PAY` bit in the `FEATURE` register must be set.

7.4.2 Auto Retransmission (ART)

The auto retransmission is a function that retransmits a packet if an ACK packet is not received. It is used in an auto acknowledgement system on the PTX. When a packet is not acknowledged, you can set the number of times it is allowed to retransmit by setting the ARC bits in the `SETUP_RETR` register. PTX enters RX mode and waits a short period for an ACK packet each time a packet is transmitted. The time period the PTX is in RX mode is based on the following conditions:

- Auto Retransmit Delay (ARD) has elapsed.
- No address match within 250µs (or 500µs in 250kbps mode).
- After received packet (CRC correct or not).

nRF24L01+ asserts the TX_DS IRQ when the ACK packet is received.

nRF24L01+ enters standby-I mode if there is no more untransmitted data in the TX FIFO and the CE pin is low. If the ACK packet is not received, nRF24L01+ goes back to TX mode after a delay defined by ARD and retransmits the data. This continues until acknowledgment is received, or the maximum number of retransmits is reached.

Two packet loss counters are incremented each time a packet is lost, ARC_CNT and PLOS_CNT in the OBSERVE_TX register. The ARC_CNT counts the number of retransmissions for the current transaction. You reset ARC_CNT by initiating a new transaction. The PLOS_CNT counts the total number of retransmissions since the last channel change. You reset PLOS_CNT by writing to the RF_CH register. It is possible to use the information in the OBSERVE_TX register to make an overall assessment of the channel quality.

The ARD defines the time from the end of a transmitted packet to when a retransmit starts on the PTX. ARD is set in SETUP_RETR register in steps of 250µs. A retransmit is made if no ACK packet is received by the PTX.

There is a restriction on the length of ARD when using ACK packets with payload. The ARD time must never be shorter than the sum of the startup time and the time on-air for the ACK packet:

- For 2Mbps data rate and 5 byte address; 15 byte is maximum ACK packet payload length for ARD=250µs (reset value).
- For 1Mbps data rate and 5 byte address; 5 byte is maximum ACK packet payload length for ARD=250µs (reset value).

ARD=500µs is long enough for any ACK payload length in 1 or 2Mbps mode.

- For 250kbps data rate and 5byte address the following values apply:

ARD	ACK packet size (in bytes)
1500µs	All ACK payload sizes
1250µs	≤ 24
1000µs	≤ 16
750µs	≤ 8
500µs	Empty ACK with no payload

Table 18. Maximum ACK payload length for different retransmit delays at 250kbps

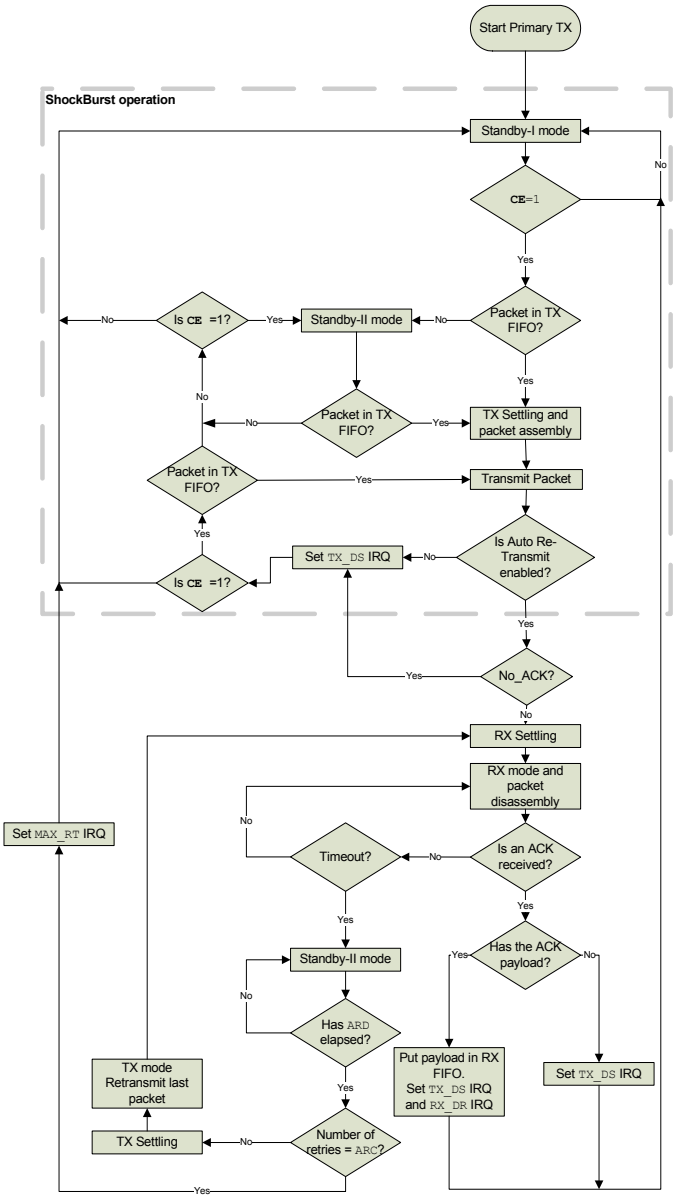
As an alternative to Auto Retransmit it is possible to manually set the nRF24L01+ to retransmit a packet a number of times. This is done by the REUSE_TX_PL command. The MCU must initiate each transmission of the packet with a pulse on the CE pin when this command is used.

7.5 Enhanced ShockBurst flowcharts

This section contains flowcharts outlining PTX and PRX operation in Enhanced ShockBurst™.

7.5.1 PTX operation

The flowchart in Figure 10. outlines how a nRF24L01+ configured as a PTX behaves after entering standby-I mode.



Note: ShockBurst™ operation is outlined with a dashed square.

Figure 10. PTX operations in Enhanced ShockBurst™

Activate PTX mode by setting the **CE** pin high. If there is a packet present in the TX FIFO the nRF24L01+ enters TX mode and transmits the packet. If Auto Retransmit is enabled, the state machine checks if the NO_ACK flag is set. If it is not set, the nRF24L01+ enters RX mode to receive an ACK packet. If the received ACK packet is empty, only the TX_DS IRQ is asserted. If the ACK packet contains a payload, both TX_DS IRQ and RX_DR IRQ are asserted simultaneously before nRF24L01+ returns to standby-I mode.

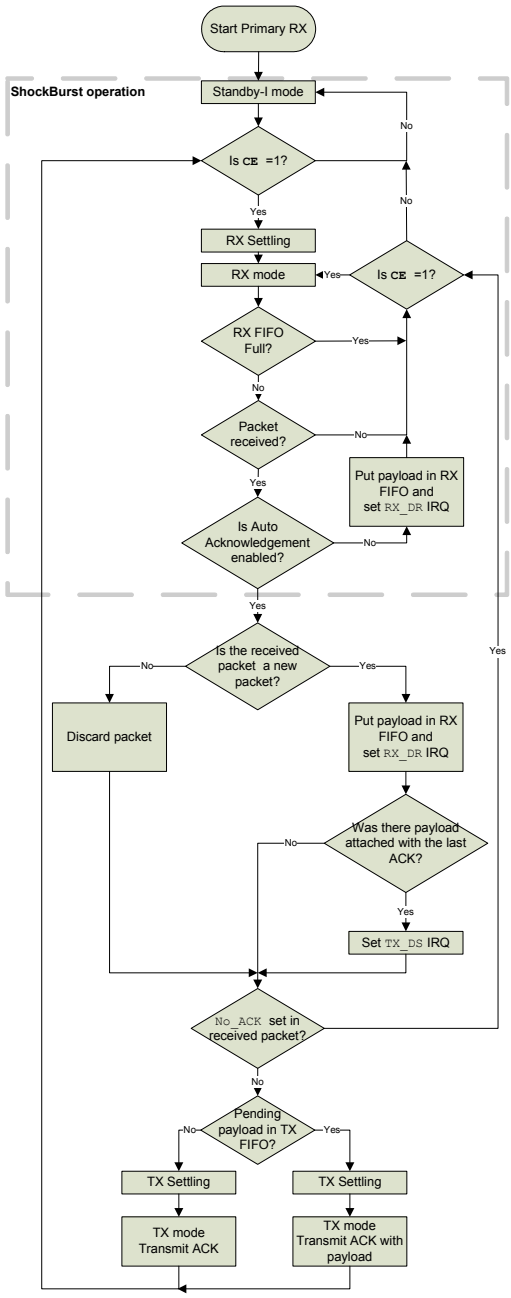
If the ACK packet is not received before timeout occurs, the nRF24L01+ returns to standby-II mode. It stays in standby-II mode until the ARD has elapsed. If the number of retransmits has not reached the ARC, the nRF24L01+ enters TX mode and transmits the last packet once more.

While executing the Auto Retransmit feature, the number of retransmits can reach the maximum number defined in ARC. If this happens, the nRF24L01+ asserts the MAX_RT IRQ and returns to standby-I mode.

If the **CE** is high and the TX FIFO is empty, the nRF24L01+ enters Standby-II mode.

7.5.2 PRX operation

The flowchart in Figure 11. outlines how a nRF24L01+ configured as a PRX behaves after entering standby-I mode.



Note: ShockBurst™ operation is outlined with a dashed square.

Figure 11. PRX operations in Enhanced ShockBurst™

Activate PRX mode by setting the **CE** pin high. The nRF24L01+ enters RX mode and starts searching for packets. If a packet is received and Auto Acknowledgement is enabled, nRF24L01+ decides if the packet is new or a copy of a previously received packet. If the packet is new the payload is made available in the

RX FIFO and the RX_DR IRQ is asserted. If the last received packet from the transmitter is acknowledged with an ACK packet with payload, the TX_DS IRQ indicates that the PTX received the ACK packet with payload. If the No_ACK flag is not set in the received packet, the PRX enters TX mode. If there is a pending payload in the TX FIFO it is attached to the ACK packet. After the ACK packet is transmitted, the nRF24L01+ returns to RX mode.

A copy of a previously received packet might be received if the ACK packet is lost. In this case, the PRX discards the received packet and transmits an ACK packet before it returns to RX mode.

7.6 MultiCeiver™

MultiCeiver™ is a feature used in RX mode that contains a set of six parallel data pipes with unique addresses. A data pipe is a logical channel in the physical RF channel. Each data pipe has its own physical address (data pipe address) decoding in the nRF24L01+.

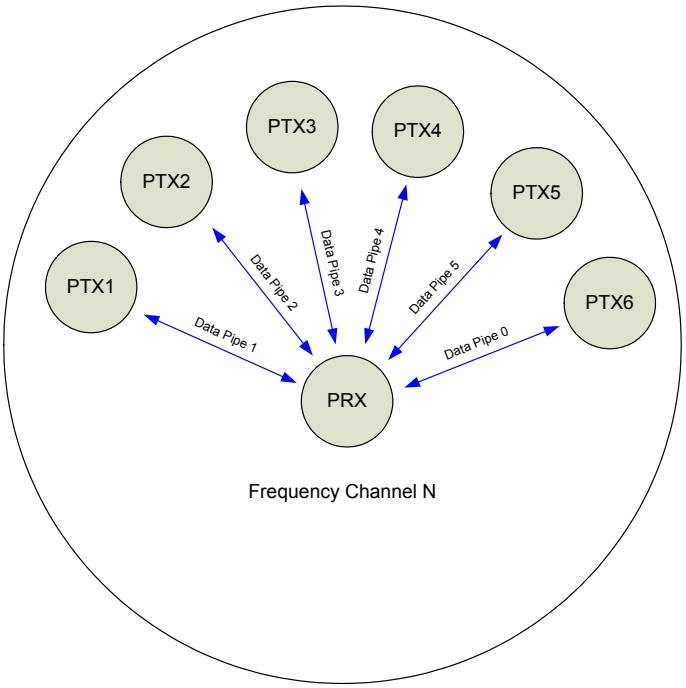


Figure 12. PRX using MultiCeiver™

nRF24L01+ configured as PRX (primary receiver) can receive data addressed to six different data pipes in one frequency channel as shown in Figure 12. Each data pipe has its own unique address and can be configured for individual behavior.

Up to six nRF24L01+s configured as PTX can communicate with one nRF24L01+ configured as a PRX. All data pipe addresses are searched for simultaneously. Only one data pipe can receive a packet at a time. All data pipes can perform Enhanced ShockBurst™ functionality.

The following settings are common to all data pipes:

- CRC enabled/disabled (CRC always enabled when Enhanced ShockBurst™ is enabled)
- CRC encoding scheme
- RX address width
- Frequency channel
- Air data rate
- LNA gain

The data pipes are enabled with the bits in the `EN_RXADDR` register. By default only data pipe 0 and 1 are enabled. Each data pipe address is configured in the `RX_ADDR_PX` registers.

Note: Always ensure that none of the data pipes have the same address.

Each pipe can have up to a 5 byte configurable address. Data pipe 0 has a unique 5 byte address. Data pipes 1-5 share the four most significant address bytes. The LSByte must be unique for all six pipes. Figure 13. is an example of how data pipes 0-5 are addressed.

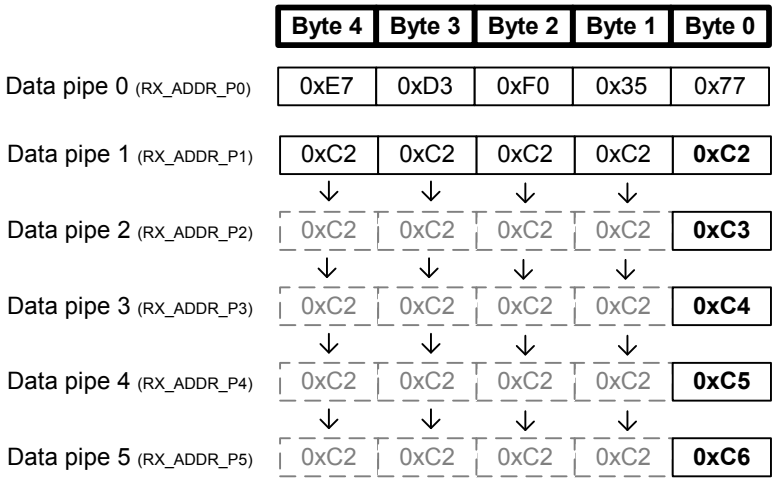


Figure 13. Addressing data pipes 0-5

The PRX, using MultiCeiver™ and Enhanced ShockBurst™, receives packets from more than one PTX. To ensure that the ACK packet from the PRX is transmitted to the correct PTX, the PRX takes the data pipe address where it received the packet and uses it as the TX address when transmitting the ACK packet. Figure 14. is an example of an address configuration for the PRX and PTX. On the PRX the `RX_ADDR_Pn`, defined as the pipe address, must be unique. On the PTX the `TX_ADDR` must be the same as the `RX_ADDR_P0` and as the pipe address for the designated pipe.

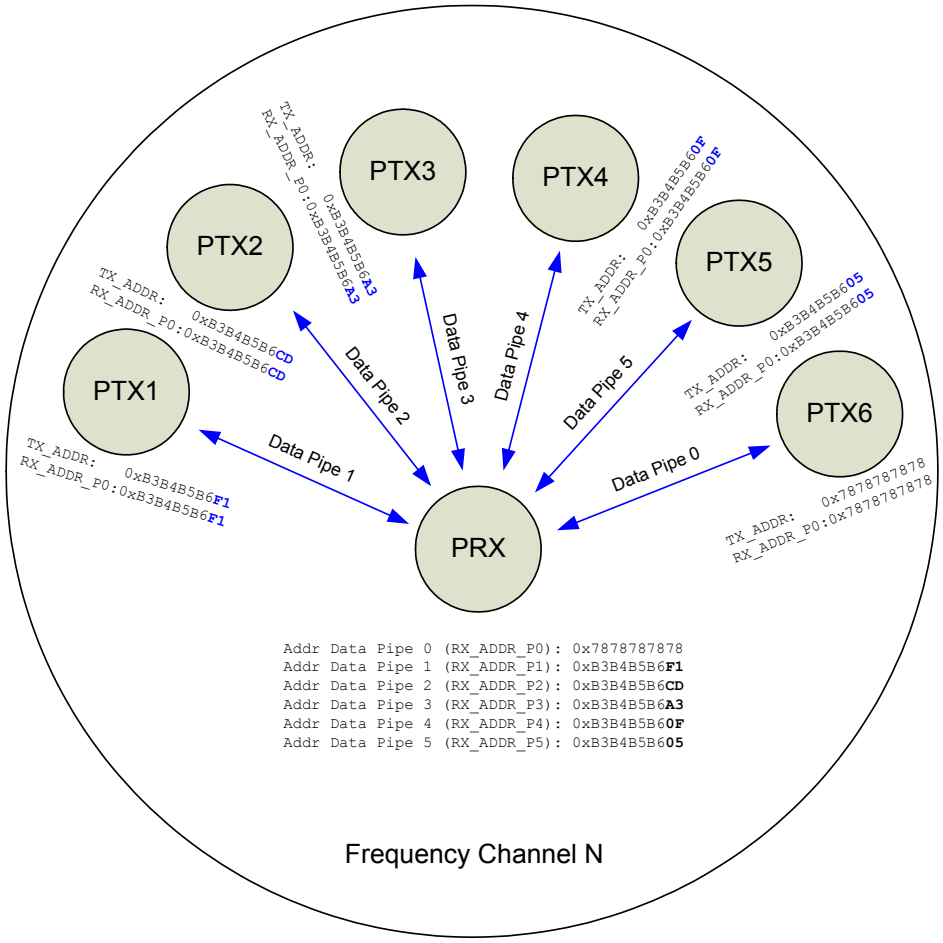
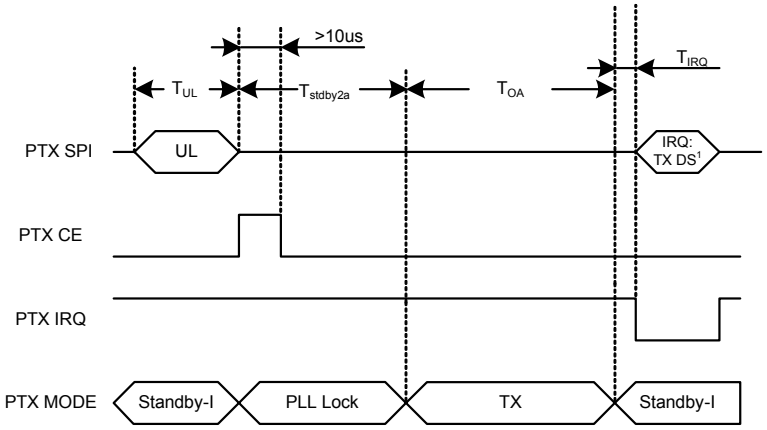


Figure 14. Example of data pipe addressing in MultiCeiver™

Only when a data pipe receives a complete packet can other data pipes begin to receive data. When multiple PTXs are transmitting to a PRX, the ARD can be used to skew the auto retransmission so that they only block each other once.

7.7 Enhanced ShockBurst™ timing

This section describes the timing sequence of Enhanced ShockBurst™ and how all modes are initiated and operated. The Enhanced ShockBurst™ timing is controlled through the Data and Control interface. The nRF24L01+ can be set to static modes or autonomous modes where the internal state machine controls the events. Each autonomous mode/sequence ends with an interrupt at the **IRQ** pin. All the interrupts are indicated as IRQ events in the timing diagrams.



1 IRQ if No Ack is on.

T_{IRQ} = 8.2µs @ 1Mbps, T_{IRQ} = 6.0µs @ 2Mbps, $T_{stdby2a}$ = 130us

Figure 15. Transmitting one packet with NO_ACK on

The following equations calculate various timing measurements:

Symbol	Description	Equation
T_{OA}	Time on-air	$T_{OA} = \frac{packet\ length}{air\ data\ rate} = \frac{8\left[\frac{bit}{byte}\right]\cdot\left(1[byte]_{preamble} + 3,4\ or\ 5[bytes]_{address} + N[bytes]_{payload} + 1\ or\ 2[bytes]_{CRC}\right) + 9[bit]_{packet\ control\ field}}{air\ data\ rate\left[\frac{bit}{s}\right]}$
T_{ACK}	Time on-air Ack	$T_{ACK} = \frac{packet\ length}{air\ data\ rate} = \frac{8\left[\frac{bit}{byte}\right]\cdot\left(1[byte]_{preamble} + 3,4\ or\ 5[bytes]_{address} + N[bytes]_{payload} + 1\ or\ 2[bytes]_{CRC}\right) + 9[bit]_{packet\ control\ field}}{air\ data\ rate\left[\frac{bit}{s}\right]}$
T_{UL}	Time Upload	$T_{UL} = \frac{payload\ length}{SPI\ data\ rate} = \frac{8\left[\frac{bit}{byte}\right]\cdot N[bytes]_{payload}}{SPI\ data\ rate\left[\frac{bit}{s}\right]}$
T_{ESB}	Time Enhanced ShockBurst™ cycle	$T_{ESB} = T_{UL} + 2\ .\ T_{stby2a} + T_{OA} + T_{ACK} + T_{IRQ}$

Table 19. Timing equations

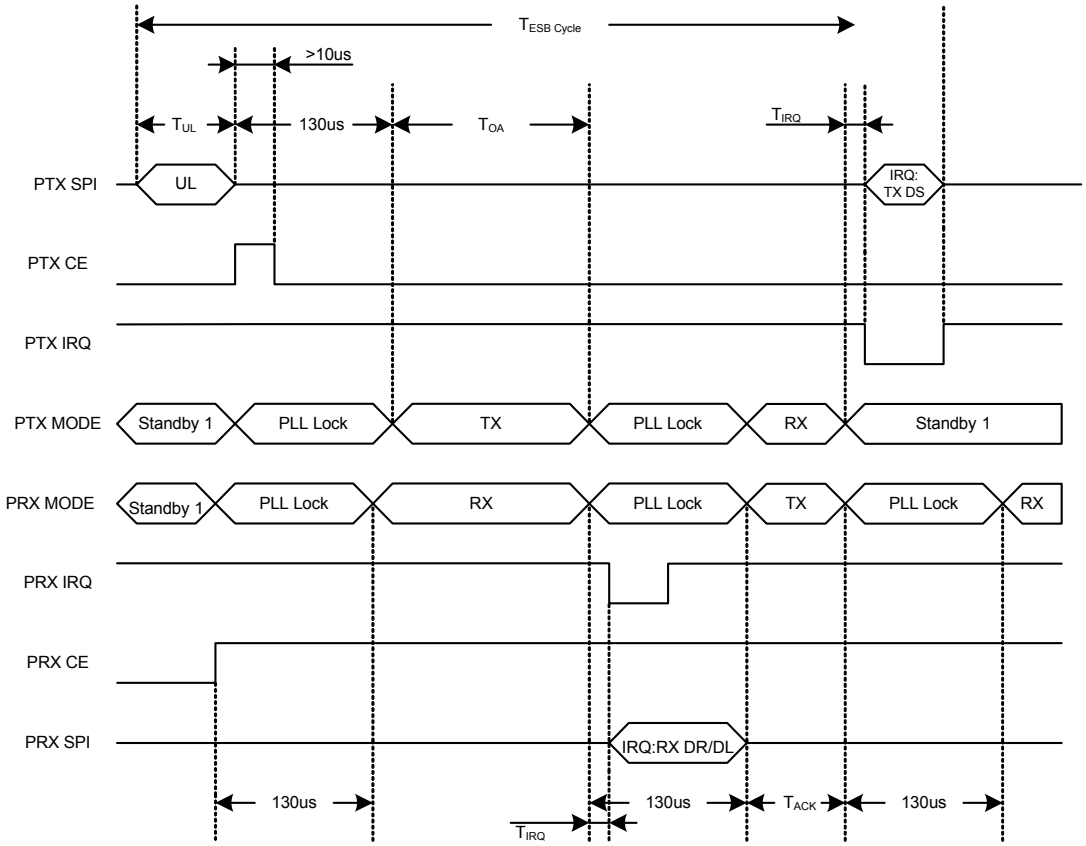


Figure 16. Timing of Enhanced ShockBurst™ for one packet upload (2Mbps)

In Figure 16. the transmission and acknowledgement of a packet is shown. The PRX device activates RX mode (**CE**=1), and the PTX device is activated in TX mode (**CE**=1 for minimum 10µs). After 130µs the transmission starts and finishes after the elapse of T_{OA}.

When the transmission ends the PTX device automatically switches to RX mode to wait for the ACK packet from the PRX device. When the PRX device receives the packet it sets the interrupt for the host MCU and switches to TX mode to send an ACK. After the PTX device receives the ACK packet it sets the interrupt to the MCU and clears the packet from the TX FIFO.

In Figure 17. the PTX timing of a packet transmission is shown when the first ACK packet is lost. To see the complete transmission when the ACK packet fails see Figure 20. on page 46.

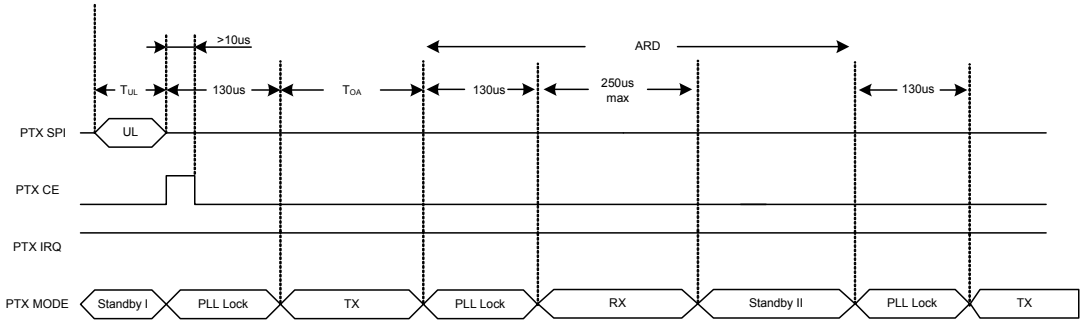


Figure 17. Timing of Enhanced ShockBurst™ when the first ACK packet is lost (2Mbps)

7.8 Enhanced ShockBurst™ transaction diagram

This section describes several scenarios for the Enhanced ShockBurst™ automatic transaction handling. The call outs in this section's figures indicate the IRQs and other events. For MCU activity the event may be placed at a different timeframe.

Note: The figures in this section indicate the earliest possible download (DL) of the packet to the MCU and the latest possible upload (UL) of payload to the transmitter.

7.8.1 Single transaction with ACK packet and interrupts

In Figure 18. the basic auto acknowledgement is shown. After the packet is transmitted by the PTX and received by the PRX the ACK packet is transmitted from the PRX to the PTX. The `RX_DR` IRQ is asserted after the packet is received by the PRX, whereas the `TX_DS` IRQ is asserted when the packet is acknowledged and the ACK packet is received by the PTX.

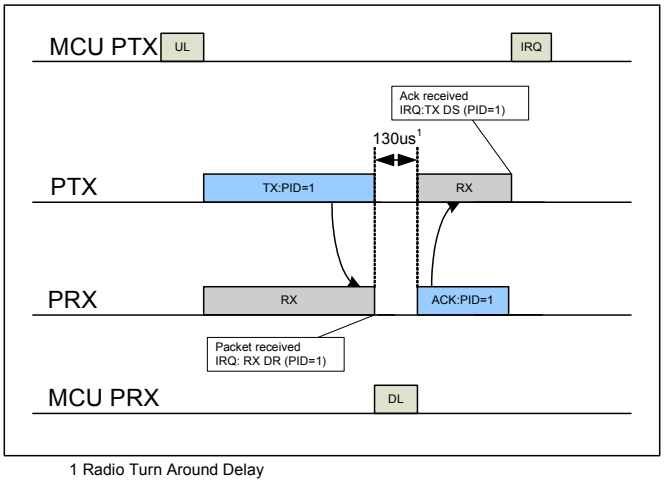


Figure 18. TX/RX cycles with ACK and the according interrupts

7.8.2 Single transaction with a lost packet

Figure 19. is a scenario where a retransmission is needed due to loss of the first packet transmit. After the packet is transmitted, the PTX enters RX mode to receive the ACK packet. After the first transmission, the PTX waits a specified time for the ACK packet, if it is not in the specific time slot the PTX retransmits the packet as shown in Figure 19.

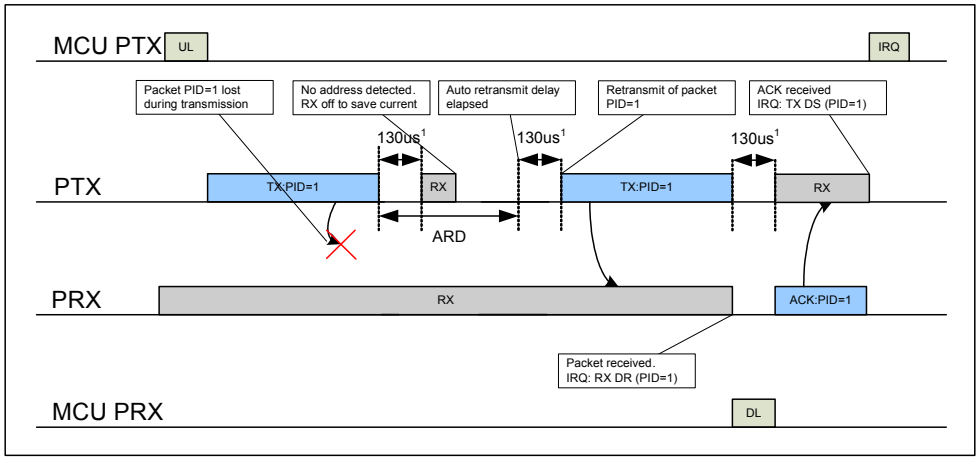


Figure 19. TX/RX cycles with ACK and the according interrupts when the first packet transmit fails

When an address is detected the PTX stays in RX mode until the packet is received. When the retransmitted packet is received by the PRX (see Figure 19.), the `RX_DR` IRQ is asserted and an ACK is transmitted back to the PTX. When the ACK is received by the PTX, the `TX_DS` IRQ is asserted.

7.8.3 Single transaction with a lost ACK packet

Figure 20. is a scenario where a retransmission is needed after a loss of the ACK packet. The corresponding interrupts are also indicated.

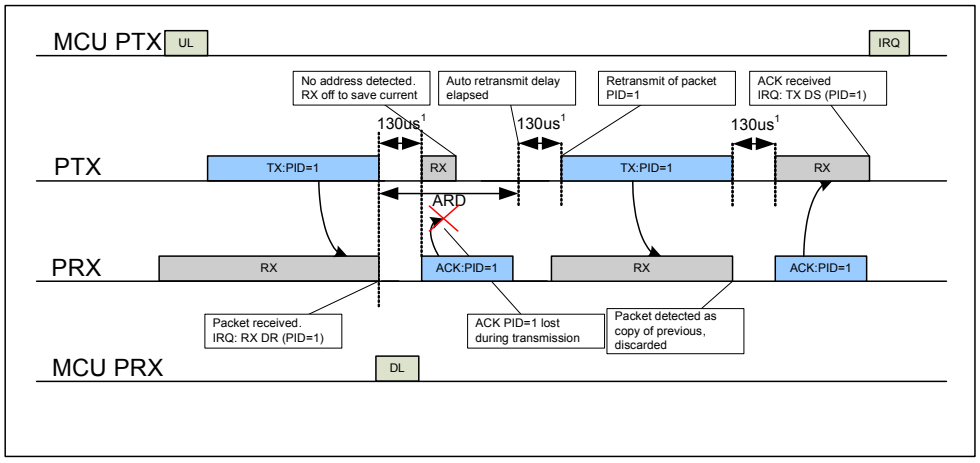
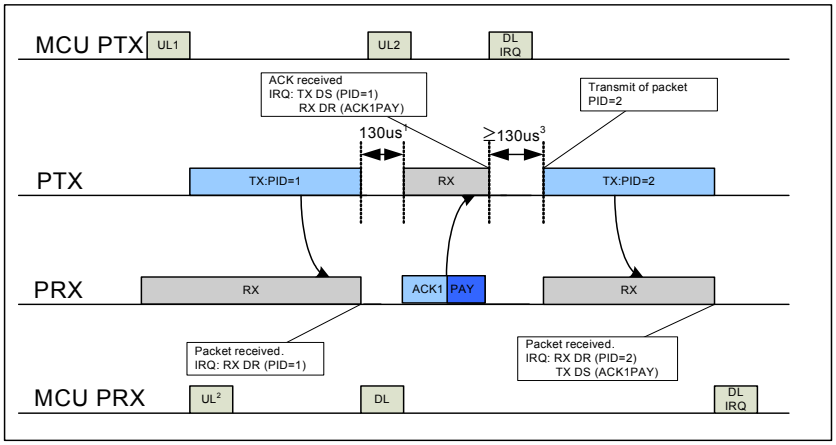


Figure 20. TX/RX cycles with ACK and the according interrupts when the ACK packet fails

7.8.4 Single transaction with ACK payload packet

Figure 21. is a scenario of the basic auto acknowledgement with payload. After the packet is transmitted by the PTX and received by the PRX the ACK packet with payload is transmitted from the PRX to the PTX. The RX_DR IRQ is asserted after the packet is received by the PRX, whereas on the PTX side the TX_DS IRQ is asserted when the ACK packet is received by the PTX. On the PRX side, the TX_DS IRQ for the ACK packet payload is asserted after a new packet from PTX is received. The position of the IRQ in Figure 21. shows where the MCU can respond to the interrupt.

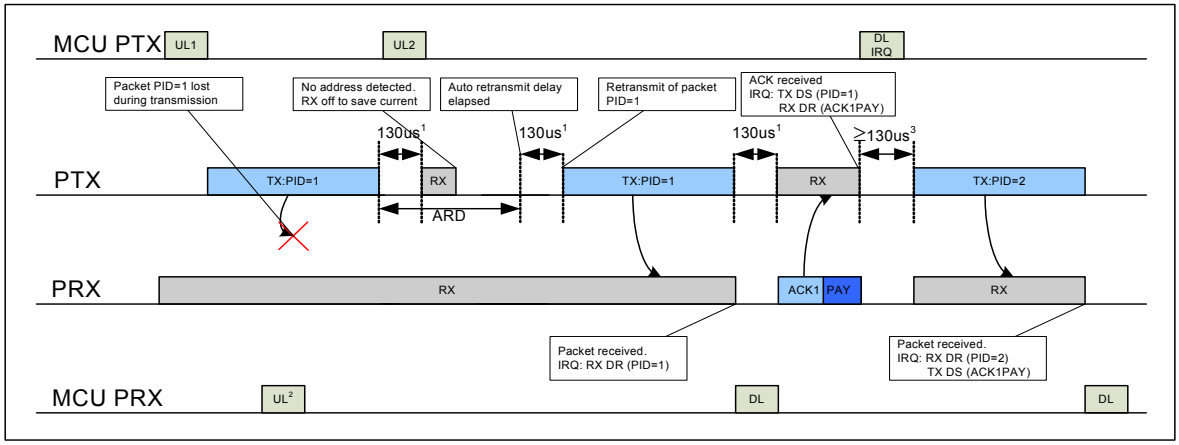


1 Radio Turn Around Delay
2 Uploading Payload for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

Figure 21. TX/RX cycles with ACK Payload and the according interrupts

7.8.5 Single transaction with ACK payload packet and lost packet

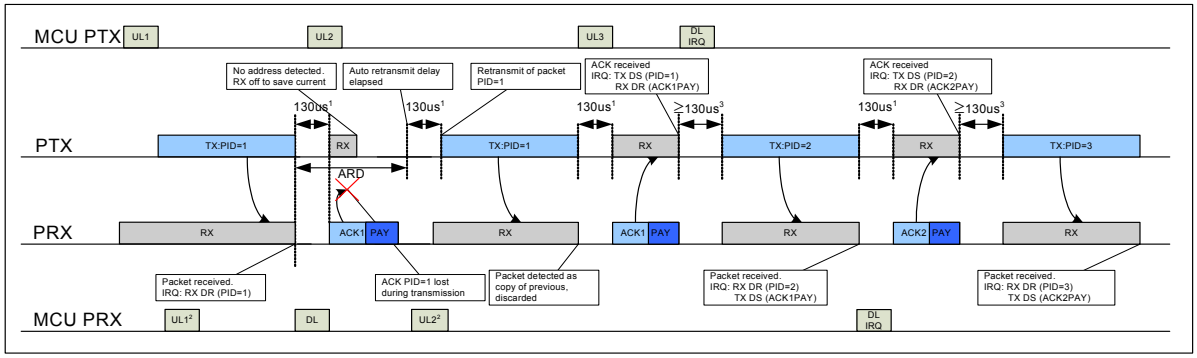
Figure 22. is a scenario where the first packet is lost and a retransmission is needed before the RX_DR IRQ on the PRX side is asserted. For the PTX both the TX_DS and RX_DR IRQ are asserted after the ACK packet is received. After the second packet (PID=2) is received on the PRX side both the RX_DR (PID=2) and TX_DS (ACK packet payload) IRQ are asserted.



1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

Figure 22. TX/RX cycles and the according interrupts when the packet transmission fails

7.8.6 Two transactions with ACK payload packet and the first ACK packet lost

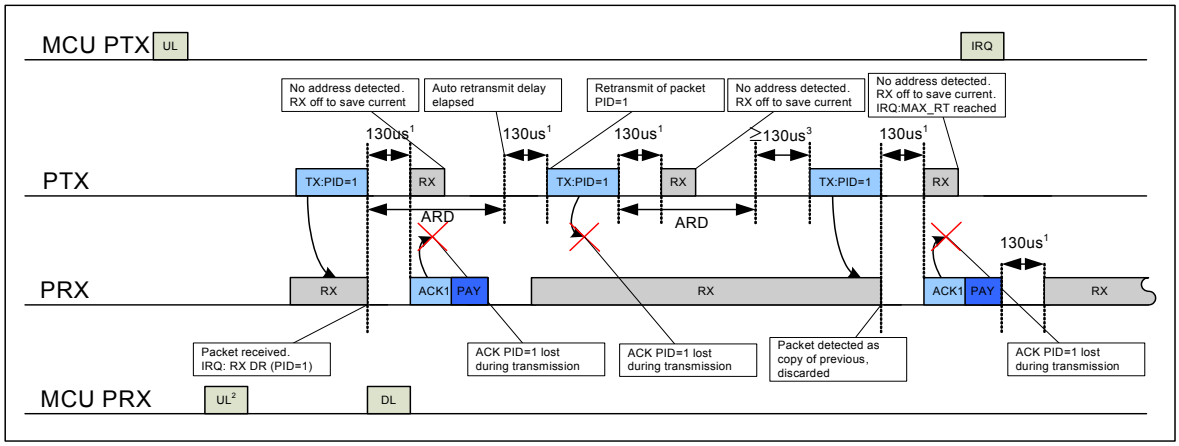


1 Radio Turn Around Delay
2 Uploading Payload for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

Figure 23. TX/RX cycles with ACK Payload and the according interrupts when the ACK packet fails

In Figure 23. the ACK packet is lost and a retransmission is needed before the TX_DS IRQ is asserted, but the RX_DR IRQ is asserted immediately. The retransmission of the packet (PID=1) results in a discarded packet. For the PTX both the TX_DS and RX_DR IRQ are asserted after the second transmission of ACK, which is received. After the second packet (PID=2) is received on the PRX both the RX_DR (PID=2) and TX_DS (ACK1PAY) IRQ is asserted. The callouts explains the different events and interrupts.

7.8.7 Two transactions where max retransmissions is reached



1 Radio Turn Around Delay
2 Uploading Paylod for Ack Packet
3 Delay defined by MCU on PTX side, ≥ 130us

Figure 24. TX/RX cycles with ACK Payload and the according interrupts when the transmission fails. ARC is set to 2.

MAX_RT IRQ is asserted if the auto retransmit counter (ARC_CNT) exceeds the programmed maximum limit (ARC). In Figure 24. the packet transmission ends with a MAX_RT IRQ. The payload in TX FIFO is NOT removed and the MCU decides the next step in the protocol. A toggle of the **CE** starts a new transmitting sequence of the same packet. The payload can be removed from the TX FIFO using the FLUSH_TX command.

7.9 Compatibility with ShockBurst™

You must disable Enhanced ShockBurst™ for backward compatibility with the nRF2401A, nRF2402, nRF24E1 and nRF24E2. Set the register `EN_AA` = 0x00 and `ARC` = 0 to disable Enhanced ShockBurst™. In addition, the nRF24L01+ air data rate must be set to 1Mbps or 250kbps.

7.9.1 ShockBurst™ packet format

Figure 25. shows the packet format with MSB to the left.

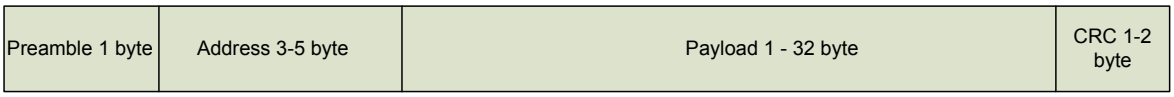


Figure 25. A ShockBurst™ packet compatible with nRF2401/nRF2402/nRF24E1/nRF24E2 devices.

The ShockBurst™ packet format has a preamble, address, payload and CRC field that are the same as the Enhanced ShockBurst™ packet format described in section 7.3 on page 28.

The differences between the ShockBurst™ packet and the Enhanced ShockBurst™ packet are:

- The 9 bit Packet Control Field is not present in the ShockBurst™ packet format.
- The CRC is optional in the ShockBurst™ packet format and is controlled by the `EN_CRC` bit in the `CONFIG` register.

8 Data and Control Interface

The data and control interface gives you access to all the features in the nRF24L01+. The data and control interface consists of the following six 5Volt tolerant digital signals:

- **IRQ** (this signal is active low and controlled by three maskable interrupt sources)
- **CE** (this signal is active high and used to activate the chip in RX or TX mode)
- **CSN** (SPI signal)
- **SCK** (SPI signal)
- **MOSI** (SPI signal)
- **MISO** (SPI signal)

Using 1 byte SPI commands, you can activate the nRF24L01+ data FIFOs or the register map during all modes of operation.

8.1 Features

- Special SPI commands for quick access to the most frequently used features
- 0-10Mbps 4-wire SPI
- 8 bit command set
- Easily configurable register map
- Full three level FIFO for both TX and RX direction

8.2 Functional description

The SPI is a standard SPI with a maximum data rate of 10Mbps.

8.3 SPI operation

This section describes the SPI commands and timing.

8.3.1 SPI commands

The SPI commands are shown in Table 20. Every new command must be started by a high to low transition on **CSN**.

The STATUS register is serially shifted out on the **MISO** pin simultaneously to the SPI command word shifting to the **MOSI** pin.

The serial shifting SPI commands is in the following format:

<**Command word**: MSBit to LSBit (one byte)>

<**Data bytes**: LSByte to MSByte, MSBit in each byte first>

See Figure 26. on page 52 and Figure 27. on page 52 for timing information.

Command name	Command word (binary)	# Data bytes	Operation
R_REGISTER	000A AAAA	1 to 5 LSByte first	Read command and status registers. AAAAA = 5 bit Register Map Address
W_REGISTER	001A AAAA	1 to 5 LSByte first	Write command and status registers. AAAAA = 5 bit Register Map Address Executable in power down or standby modes only.
R_RX_PAYLOAD	0110 0001	1 to 32 LSByte first	Read RX-payload: 1 – 32 bytes. A read operation always starts at byte 0. Payload is deleted from FIFO after it is read. Used in RX mode.
W_TX_PAYLOAD	1010 0000	1 to 32 LSByte first	Write TX-payload: 1 – 32 bytes. A write operation always starts at byte 0 used in TX payload.
FLUSH_TX	1110 0001	0	Flush TX FIFO, used in TX mode
FLUSH_RX	1110 0010	0	Flush RX FIFO, used in RX mode Should not be executed during transmission of acknowledge, that is, acknowledge package will not be completed.
REUSE_TX_PL	1110 0011	0	Used for a PTX device Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX payload reuse must not be activated or deactivated during package transmission.
R_RX_PL_WID[a]	0110 0000	1	Read RX payload width for the top R_RX_PAYLOAD in the RX FIFO. **Note:** Flush RX FIFO if the read value is larger than 32 bytes.
W_ACK_PAYLOAD[a]	1010 1PPP	1 to 32 LSByte first	Used in RX mode. Write Payload to be transmitted together with ACK packet on PIPE PPP. (PPP valid in the range from 000 to 101). Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled using first in - first out principle. Write payload: 1– 32 bytes. A write operation always starts at byte 0.
W_TX_PAYLOAD_NOACK[a]	1011 0000	1 to 32 LSByte first	Used in TX mode. Disables AUTOACK on this specific packet.
NOP	1111 1111	0	No Operation. Might be used to read the STATUS register

a. The bits in the FEATURE register shown in Table 28. on page 63 have to be set.

Table 20. Command set for the nRF24L01+ SPI

The W_REGISTER and R_REGISTER commands operate on single or multi-byte registers. When accessing multi-byte registers read or write to the MSBit of LSByte first. You can terminate the writing before all bytes in a multi-byte register are written, leaving the unwritten MSByte(s) unchanged. For example, the LSByte of RX_ADDR_P0 can be modified by writing only one byte to the RX_ADDR_P0 register. The content of the status register is always read to **MISO** after a high to low transition on **CSN**.

Note: The 3 bit pipe information in the STATUS register is updated during the **IRQ** pin high to low transition. The pipe information is unreliable if the STATUS register is read during an **IRQ** pin high to low transition.

8.3.2 SPI timing

SPI operation and timing is shown in Figure 26. to Figure 28. and in Table 22. to Table 27.. nRF24L01+ must be in a standby or power down mode before writing to the configuration registers.

In Figure 26. to Figure 28. the following abbreviations are used:

Abbreviation	Description
Cn	SPI command bit
Sn	STATUS register bit
Dn	Data Bit (**Note:** LSByte to MSByte, MSBit in each byte first)

Table 21. Abbreviations used in Figure 26. to Figure 28.

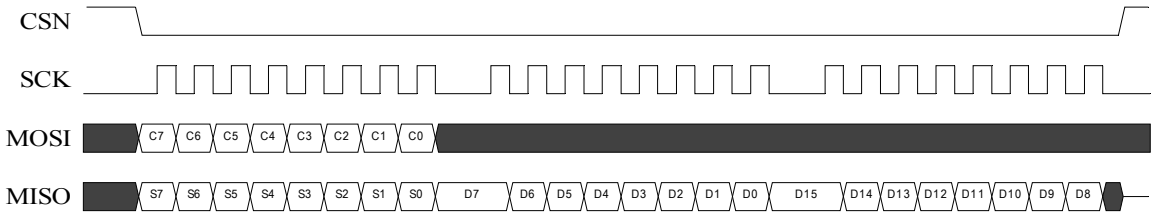


Figure 26. SPI read operation

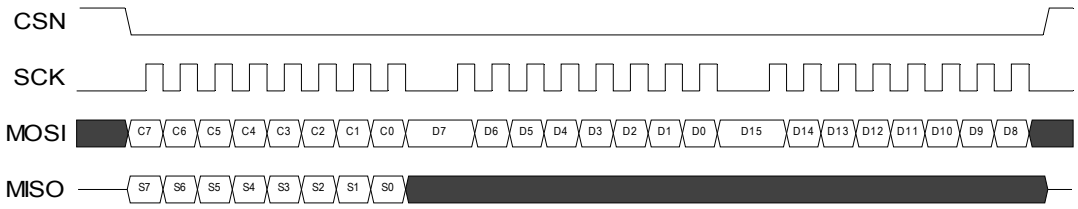


Figure 27. SPI write operation

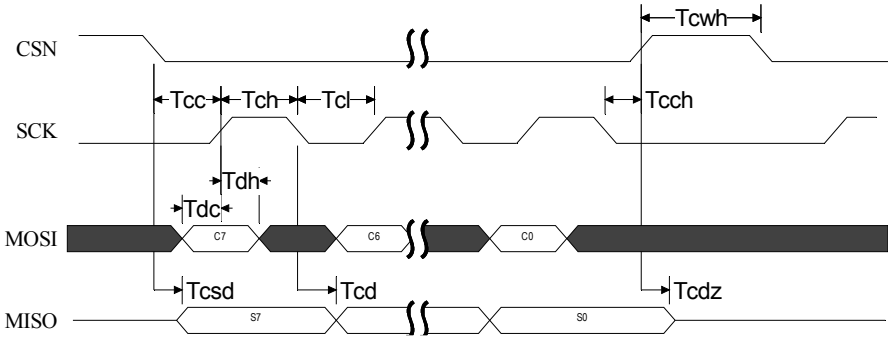


Figure 28. SPI NOP timing diagram

Figure 29. shows the R_{pull} and C_{load} that are referenced in Table 22. to Table 27.

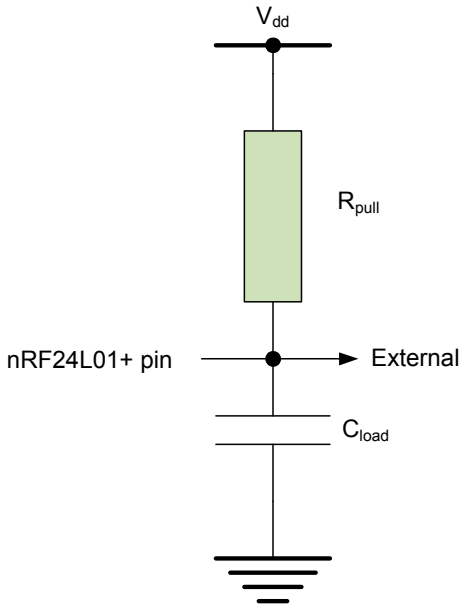


Figure 29. R_{pull} and C_{load}

Symbol	Parameters	Min.	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		38	ns
Tcd	SCK to Data Valid		55	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	10	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		38	ns

Table 22. SPI timing parameters (C_{load} = 5pF)

Symbol	Parameters	Min.	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		42	ns
Tcd	SCK to Data Valid		58	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	8	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns

Symbol	Parameters	Min.	Max	Units
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		42	ns

Table 23. SPI timing parameters (C_{load} = 10pF)

Symbol	Parameters	Min.	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		75	ns
Tcd	SCK to Data Valid		86	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	5	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		75	ns

Table 24. SPI timing parameters (R_{pull} = 10kΩ, C_{load} = 50pF)

Symbol	Parameters	Min.	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		116	ns
Tcd	SCK to Data Valid		123	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	4	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		116	ns

Table 25. SPI timing parameters (R_{pull} = 10kΩ, C_{load} = 100pF)

Symbol	Parameters	Min.	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		75	ns
Tcd	SCK to Data Valid		85	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	5	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		75	ns

Table 26. SPI timing parameters (R_{pull} = 50kΩ, C_{load} = 50pF)

Symbol	Parameters	Min.	Max	Units
Tdc	Data to SCK Setup	2		ns
Tdh	SCK to Data Hold	2		ns
Tcsd	CSN to Data Valid		116	ns
Tcd	SCK to Data Valid		121	ns
Tcl	SCK Low Time	40		ns
Tch	SCK High Time	40		ns
Fsck	SCK Frequency	0	4	MHz
Tr,Tf	SCK Rise and Fall		100	ns
Tcc	CSN to SCK Setup	2		ns
Tcch	SCK to CSN Hold	2		ns
Tcwh	CSN Inactive time	50		ns
Tcdz	CSN to Output High Z		116	ns

Table 27. SPI timing parameters (R_{pull} = 50kΩ, C_{load} = 100pF)

8.4 Data FIFO

The data FIFOs store transmitted payloads (TX FIFO) or received payloads that are ready to be clocked out (RX FIFO). The FIFOs are accessible in both PTX mode and PRX mode.

The following FIFOs are present in nRF24L01+:

- TX three level, 32 byte FIFO
- RX three level, 32 byte FIFO

Both FIFOs have a controller and are accessible through the SPI by using dedicated SPI commands. A TX FIFO in PRX can store payloads for ACK packets to three different PTX devices. If the TX FIFO contains more than one payload to a pipe, payloads are handled using the first in - first out principle. The TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to the PTX is lost. In this case, the MCU can flush the TX FIFO using the `FLUSH_TX` command.

The RX FIFO in PRX can contain payloads from up to three different PTX devices and a TX FIFO in PTX can have up to three payloads stored.

You can write to the TX FIFO using these three commands; W_TX_PAYLOAD and W_TX_PAYLOAD_NO_ACK in PTX mode and W_ACK_PAYLOAD in PRX mode. All three commands provide access to the TX_PLD register (see Table 28. on page 63. for details of this register).

The RX FIFO can be read by the command R_RX_PAYLOAD in PTX and PRX mode. This command provides access to the RX_PLD register.

The payload in TX FIFO in a PTX is not removed if the MAX_RT IRQ is asserted.

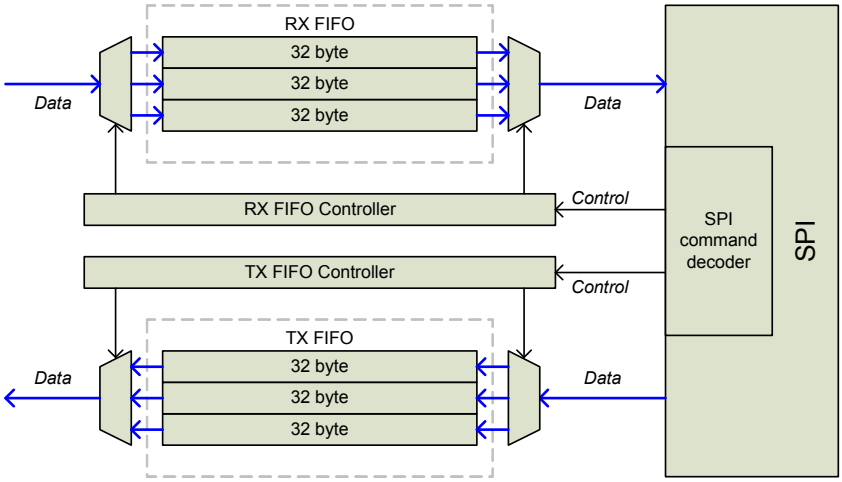


Figure 30. FIFO (RX and TX) block diagram

You can read if the TX and RX FIFO are full or empty in the FIFO_STATUS register.

8.5 Interrupt

The nRF24L01+ has an active low interrupt (**IRQ**) pin. The **IRQ** pin is activated when TX_DS IRQ, RX_DR IRQ or MAX_RT IRQ are set high by the state machine in the STATUS register. The **IRQ** pin resets when MCU writes '1' to the IRQ source bit in the STATUS register. The IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the **IRQ** pin. By setting one of the MASK bits high, the corresponding IRQ source is disabled. By default all IRQ sources are enabled.

Note: The 3 bit pipe information in the STATUS register is updated during the **IRQ** pin high to low transition. The pipe information is unreliable if the STATUS register is read during an **IRQ** pin high to low transition.

9 Register Map

You can configure and control the radio by accessing the register map through the SPI.

9.1 Register map table

All undefined bits in the table below are redundant. They are read out as '0'.

Note: Addresses 18 to 1B are reserved for test purposes, altering them makes the chip malfunction.

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
00	CONFIG				Configuration Register
	Reserved	7	0	R/W	Only '0' allowed
	MASK_RX_DR	6	0	R/W	Mask interrupt caused by RX_DR 1: Interrupt not reflected on the **IRQ** pin 0: Reflect RX_DR as active low interrupt on the **IRQ** pin
	MASK_TX_DS	5	0	R/W	Mask interrupt caused by TX_DS 1: Interrupt not reflected on the **IRQ** pin 0: Reflect TX_DS as active low interrupt on the **IRQ** pin
	MASK_MAX_RT	4	0	R/W	Mask interrupt caused by MAX_RT 1: Interrupt not reflected on the **IRQ** pin 0: Reflect MAX_RT as active low interrupt on the **IRQ** pin
	EN_CRC	3	1	R/W	Enable CRC. Forced high if one of the bits in the EN_AA is high
	CRCO	2	0	R/W	CRC encoding scheme '0' - 1 byte '1' – 2 bytes
	PWR_UP	1	0	R/W	1: POWER UP, 0:POWER DOWN
	PRIM_RX	0	0	R/W	RX/TX control 1: PRX, 0: PTX
01	EN_AA Enhanced ShockBurst™				Enable 'Auto Acknowledgment' Function Disable this functionality to be compatible with nRF2401, see page 75
	Reserved	7:6	00	R/W	Only '00' allowed
	ENAA_P5	5	1	R/W	Enable auto acknowledgement data pipe 5
	ENAA_P4	4	1	R/W	Enable auto acknowledgement data pipe 4
	ENAA_P3	3	1	R/W	Enable auto acknowledgement data pipe 3
	ENAA_P2	2	1	R/W	Enable auto acknowledgement data pipe 2
	ENAA_P1	1	1	R/W	Enable auto acknowledgement data pipe 1
	ENAA_P0	0	1	R/W	Enable auto acknowledgement data pipe 0
02	EN_RXADDR				Enabled RX Addresses
	Reserved	7:6	00	R/W	Only '00' allowed
	ERX_P5	5	0	R/W	Enable data pipe 5.
	ERX_P4	4	0	R/W	Enable data pipe 4.
	ERX_P3	3	0	R/W	Enable data pipe 3.
	ERX_P2	2	0	R/W	Enable data pipe 2.

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	ERX_P1	1	1	R/W	Enable data pipe 1.
	ERX_P0	0	1	R/W	Enable data pipe 0.
03	SETUP_AW				Setup of Address Widths (common for all data pipes)
	Reserved	7:2	000000	R/W	Only '000000' allowed
	AW	1:0	11	R/W	RX/TX Address field width '00' - Illegal '01' - 3 bytes '10' - 4 bytes '11' – 5 bytes LSByte is used if address width is below 5 bytes
04	SETUP_RETR				Setup of Automatic Retransmission
	ARD[a]	7:4	0000	R/W	Auto Retransmit Delay ‘0000’ – Wait 250µS ‘0001’ – Wait 500µS ‘0010’ – Wait 750µS …….. ‘1111’ – Wait 4000µS (Delay defined from end of transmission to start of next transmission)[b]
	ARC	3:0	0011	R/W	Auto Retransmit Count ‘0000’ –Re-Transmit disabled ‘0001’ – Up to 1 Re-Transmit on fail of AA …… ‘1111’ – Up to 15 Re-Transmit on fail of AA
05	RF_CH				RF Channel
	Reserved	7	0	R/W	Only '0' allowed
	RF_CH	6:0	0000010	R/W	Sets the frequency channel nRF24L01+ operates on
06	RF_SETUP				RF Setup Register
	CONT_WAVE	7	0	R/W	Enables continuous carrier transmit when high.
	Reserved	6	0	R/W	Only '0' allowed
	RF_DR_LOW	5	0	R/W	Set RF Data Rate to 250kbps. See RF_DR_HIGH for encoding.
	PLL_LOCK	4	0	R/W	Force PLL lock signal. Only used in test
	RF_DR_HIGH	3	1	R/W	Select between the high speed data rates. This bit is don’t care if RF_DR_LOW is set. Encoding: [RF_DR_LOW, RF_DR_HIGH]: ‘00’ – 1Mbps ‘01’ – 2Mbps ‘10’ – 250kbps ‘11’ – Reserved

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	RF_PWR	2:1	11	R/W	Set RF output power in TX mode '00' – -18dBm '01' – -12dBm '10' – -6dBm '11' – 0dBm
	Obsolete	0			Don't care
07	STATUS				Status Register (In parallel to the SPI command word applied on the **MOSI** pin, the STATUS register is shifted serially out on the **MISO** pin)
	Reserved	7	0	R/W	Only '0' allowed
	RX_DR	6	0	R/W	Data Ready RX FIFO interrupt. Asserted when new data arrives RX FIFO[c]. Write 1 to clear bit.
	TX_DS	5	0	R/W	Data Sent TX FIFO interrupt. Asserted when packet transmitted on TX. If AUTO_ACK is activated, this bit is set high only when ACK is received. Write 1 to clear bit.
	MAX_RT	4	0	R/W	Maximum number of TX retransmits interrupt Write 1 to clear bit. If MAX_RT is asserted it must be cleared to enable further communication.
	RX_P_NO	3:1	111	R	Data pipe number for the payload available for reading from RX_FIFO 000-101: Data Pipe Number 110: Not Used 111: RX FIFO Empty
	TX_FULL	0	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
08	OBSERVE_TX				Transmit observe register
	PLOS_CNT	7:4	0	R	Count lost packets. The counter is overflow protected to 15, and discontinues at max until reset. The counter is reset by writing to RF_CH. See page 75.
	ARC_CNT	3:0	0	R	Count retransmitted packets. The counter is reset when transmission of a new packet starts. See page 75.
09	RPD				
	Reserved	7:1	000000	R	
	RPD	0	0	R	Received Power Detector. This register is called CD (Carrier Detect) in the nRF24L01. The name is different in nRF24L01+ due to the different input power level threshold for this bit. See section 6.4 on page 25.
0A	RX_ADDR_P0	39:0	0xE7E7E7E7E7	R/W	Receive address data pipe 0. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
0B	RX_ADDR_P1	39:0	0xC2C2C2C2C2	R/W	Receive address data pipe 1. 5 Bytes maximum length. (LSByte is written first. Write the number of bytes defined by SETUP_AW)
0C	RX_ADDR_P2	7:0	0xC3	R/W	Receive address data pipe 2. Only LSB. MSBytes are equal to RX_ADDR_P1[39:8]
0D	RX_ADDR_P3	7:0	0xC4	R/W	Receive address data pipe 3. Only LSB. MSBytes are equal to RX_ADDR_P1[39:8]
0E	RX_ADDR_P4	7:0	0xC5	R/W	Receive address data pipe 4. Only LSB. MSBytes are equal to RX_ADDR_P1[39:8]
0F	RX_ADDR_P5	7:0	0xC6	R/W	Receive address data pipe 5. Only LSB. MSBytes are equal to RX_ADDR_P1[39:8]
10	TX_ADDR	39:0	0xE7E7E7E7E7	R/W	Transmit address. Used for a PTX device only. (LSByte is written first) Set RX_ADDR_P0 equal to this address to handle automatic acknowledge if this is a PTX device with Enhanced ShockBurst™ enabled. See page 75.
11	RX_PW_P0				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P0	5:0	0	R/W	Number of bytes in RX payload in data pipe 0 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
12	RX_PW_P1				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P1	5:0	0	R/W	Number of bytes in RX payload in data pipe 1 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
13	RX_PW_P2				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P2	5:0	0	R/W	Number of bytes in RX payload in data pipe 2 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
14	RX_PW_P3				
	Reserved	7:6	00	R/W	Only '00' allowed

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	RX_PW_P3	5:0	0	R/W	Number of bytes in RX payload in data pipe 3 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
15	RX_PW_P4				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P4	5:0	0	R/W	Number of bytes in RX payload in data pipe 4 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
16	RX_PW_P5				
	Reserved	7:6	00	R/W	Only '00' allowed
	RX_PW_P5	5:0	0	R/W	Number of bytes in RX payload in data pipe 5 (1 to 32 bytes). 0 Pipe not used 1 = 1 byte … 32 = 32 bytes
17	FIFO_STATUS				FIFO Status Register
	Reserved	7	0	R/W	Only '0' allowed
	TX_REUSE	6	0	R	Used for a PTX device Pulse the rfce high for at least 10µs to Reuse last transmitted payload. TX payload reuse is active until W_TX_PAYLOAD or FLUSH TX is executed. TX_REUSE is set by the SPI command REUSE_TX_PL, and is reset by the SPI commands W_TX_PAYLOAD or FLUSH TX
	TX_FULL	5	0	R	TX FIFO full flag. 1: TX FIFO full. 0: Available locations in TX FIFO.
	TX_EMPTY	4	1	R	TX FIFO empty flag. 1: TX FIFO empty. 0: Data in TX FIFO.
	Reserved	3:2	00	R/W	Only '00' allowed
	RX_FULL	1	0	R	RX FIFO full flag. 1: RX FIFO full. 0: Available locations in RX FIFO.
	RX_EMPTY	0	1	R	RX FIFO empty flag. 1: RX FIFO empty. 0: Data in RX FIFO.

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
N/A	ACK_PLD	255:0	X	W	Written by separate SPI command ACK packet payload to data pipe number PPP given in SPI command. Used in RX mode only. Maximum three ACK packet payloads can be pending. Payloads with same PPP are handled first in first out.
N/A	TX_PLD	255:0	X	W	Written by separate SPI command TX data payload register 1 - 32 bytes. This register is implemented as a FIFO with three levels. Used in TX mode only.
N/A	RX_PLD	255:0	X	R	Read by separate SPI command. RX data payload register. 1 - 32 bytes. This register is implemented as a FIFO with three levels. All RX channels share the same FIFO.
1C	DYNPD				Enable dynamic payload length
	Reserved	7:6	0	R/W	Only '00' allowed
	DPL_P5	5	0	R/W	Enable dynamic payload length data pipe 5. (Requires EN_DPL and ENAA_P5)
	DPL_P4	4	0	R/W	Enable dynamic payload length data pipe 4. (Requires EN_DPL and ENAA_P4)
	DPL_P3	3	0	R/W	Enable dynamic payload length data pipe 3. (Requires EN_DPL and ENAA_P3)

Address (Hex)	Mnemonic	Bit	Reset Value	Type	Description
	DPL_P2	2	0	R/W	Enable dynamic payload length data pipe 2. (Requires EN_DPL and ENAA_P2)
	DPL_P1	1	0	R/W	Enable dynamic payload length data pipe 1. (Requires EN_DPL and ENAA_P1)
	DPL_P0	0	0	R/W	Enable dynamic payload length data pipe 0. (Requires EN_DPL and ENAA_P0)
1D	FEATURE			R/W	Feature Register
	Reserved	7:3	0	R/W	Only '00000' allowed
	EN_DPL	2	0	R/W	Enables Dynamic Payload Length
	EN_ACK_PAY[d]	1	0	R/W	Enables Payload with ACK
	EN_DYN_ACK	0	0	R/W	Enables the W_TX_PAYLOAD_NOACK command

a. Please take care when setting this parameter. If the ACK payload is more than 15 byte in 2Mbps mode the ARD must be 500µS or more, if the ACK payload is more than 5byte in 1Mbps mode the ARD must be 500µS or more. In 250kbps mode (even when the payload is not in ACK) the ARD must be 500µS or more. Please see section 7.4.2 on page 33 for more information.
b. This is the time the PTX is waiting for an ACK packet before a retransmit is made. The PTX is in RX mode for 250µS (500µS in 250kbps mode) to wait for address match. If the address match is detected, it stays in RX mode to the end of the packet, unless ARD elapses. Then it goes to standby-II mode for the rest of the specified ARD. After the ARD it goes to TX mode and then retransmits the packet.
c. The RX_DR IRQ is asserted by a new packet arrival event. The procedure for handling this interrupt should be: 1) read payload through SPI, 2) clear RX_DR IRQ, 3) read FIFO_STATUS to check if there are more payloads available in RX FIFO, 4) if there are more data in RX FIFO, repeat from step 1).
d. If ACK packet payload is activated, ACK packets have dynamic payload lengths and the Dynamic Payload Length feature should be enabled for pipe 0 on the PTX and PRX. This is to ensure that they receive the ACK packets with payloads. If the ACK payload is more than 15 byte in 2Mbps mode the ARD must be 500µS or more, and if the ACK payload is more than 5 byte in 1Mbps mode the ARD must be 500µS or more. In 250kbps mode (even when the payload is not in ACK) the ARD must be 500µS or more.

Table 28. Register map of nRF24L01+

10 Peripheral RF Information

This chapter describes peripheral circuitry and PCB layout requirements that are important for achieving optimum RF performance from the nRF24L01+.

10.1 Antenna output

The **ANT1** and **ANT2** output pins provide a balanced RF output to the antenna. The pins must have a DC path to **VDD_PA**, either through a RF choke or through the center point in a balanced dipole antenna. A load of 15Ω+j88Ω is recommended for maximum output power (0dBm). Lower load impedance (for instance, 50Ω) can be obtained by fitting a simple matching network between the load and **ANT1** and **ANT2**. A recommended matching network for 50Ω load impedance is described in chapter 11 on page 66.

10.2 Crystal oscillator

A crystal used with the nRF24L01+ must fulfil the specifications in Table 11. on page 19.

To achieve a crystal oscillator solution with low power consumption and fast start up time use a crystal with a low load capacitance specification. A lower C_0 also gives lower current consumption and faster start up time, but can increase the cost of the crystal. Typically C_0=1.5pF at a crystal specified for C_{0max}=7.0pF.

The crystal load capacitance, C_L, is given by:

$C_L = \frac{C_1' \cdot C_2'}{C_1' + C_2'}$, where $C_1' = C_1 + C_{PCB1} + C_{I1}$ and $C_2' = C_2 + C_{PCB2} + C_{I2}$

C_1 and C_2 are SMD capacitors, see the application schematics in Figure 32. on page 66. C_{PCB1} and C_{PCB2} are the layout parasitic on the circuit board. C_{I1} and C_{I2} are the internal capacitance load of the **XC1** and **XC2** pins respectively; the value is typically 1pF for both these pins.

10.3 nRF24L01+ crystal sharing with an MCU

Follow the rules described in sections 10.3.1 and 10.3.2 when using an MCU to drive the crystal reference input **XC1** of the nRF24L01+ transceiver.

10.3.1 Crystal parameters

The MCU sets the requirement of load capacitance C_L when it is driving the nRF24L01+ clock input. A frequency accuracy of ±60ppm is required to get a functional radio link. The nRF24L01+ loads the crystal by 1pF in addition to the PCB routing.

10.3.2 Input crystal amplitude and current consumption

The input signal should not have amplitudes exceeding any rail voltage. Exceeding rail voltage excites the ESD structure and consequently, the radio performance degrades below specification. You must use an external DC block if you are testing the nRF24L01+ with a reference source that has no DC offset (which is usual with a RF source).

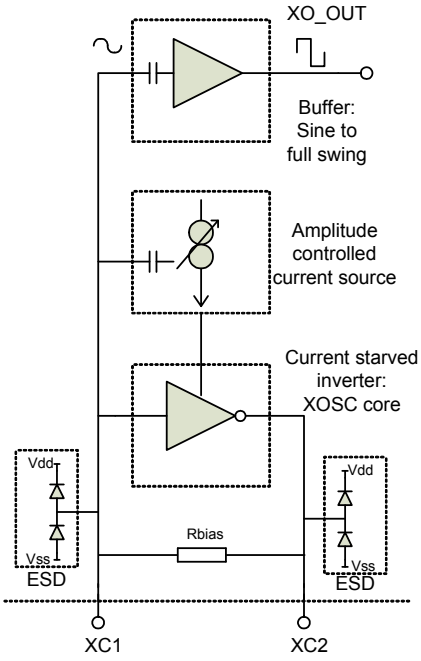


Figure 31. Principle of crystal oscillator

The nRF24L01+ crystal oscillator is amplitude regulated. It is recommended to use an input signal larger than 0.4V-peak to achieve low current consumption and good signal-to-noise ratio when using an external clock. **XC2** is not used and can be left as an open pin when clocked externally.

10.4 PCB layout and decoupling guidelines

A well designed PCB is necessary to achieve good RF performance. A poor layout can lead to loss of performance or functionality. You can download a fully qualified RF layout for the nRF24L01+ and its surrounding components, including matching networks, from www.nordicsemi.no.

A PCB with a minimum of two layers including a ground plane is recommended for optimum performance. The nRF24L01+ DC supply voltage should be decoupled as close as possible to the **VDD** pins with high performance RF capacitors, see Table 29. on page 67. Mounting a large surface mount capacitor (for example, 4.7µF ceramic) in parallel with the smaller value capacitors is recommended. The nRF24L01+ supply voltage should be filtered and routed separately from the supply voltages of any digital circuitry.

Avoid long power supply lines on the PCB. All device grounds, **VDD** connections and **VDD** bypass capacitors must be connected as close as possible to the nRF24L01+ IC. The **VSS** pins should be connected directly to the ground plane for a PCB with a topside RF ground plane. We recommend having via holes as close as possible to the **VSS** pads for a PCB with a bottom ground plane. A minimum of one via hole should be used for each **VSS** pin.

Full swing digital data or control signals should not be routed close to the crystal or the power supply lines. The exposed die attach pad is a ground pad connected to the IC substrate die ground and is intentionally not used in our layouts. We recommend to keep it unconnected.

11 Application example

nRF24L01+ with single ended matching network crystal, bias resistor, and decoupling capacitors.

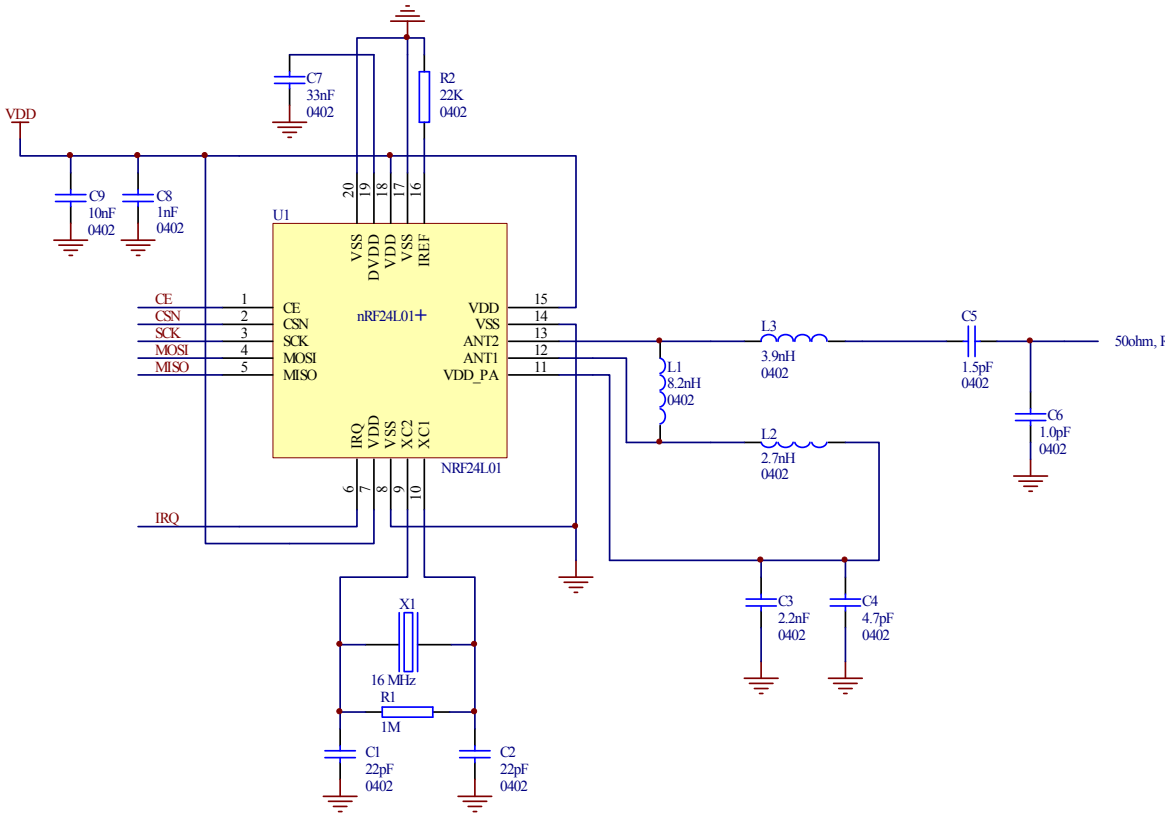


Figure 32. nRF24L01+ schematic for RF layouts with single ended 50Ω RF output

Part	Designator	Footprint	Description
22pF[a]	C1	0402	NPO, +/- 2%
22pF[a]	C2	0402	NPO, +/- 2%
2.2nF	C3	0402	X7R, +/- 10%
4.7pF	C4	0402	NPO, +/- 0.25pF
1.5pF	C5	0402	NPO, +/- 0.1pF
1,0pF	C6	0402	NPO, +/- 0.1pF
33nF	C7	0402	X7R, +/- 10%
1nF	C8	0402	X7R, +/- 10%
10nF	C9	0402	X7R, +/- 10%
8,2nH	L1	0402	chip inductor +/- 5%
2.7nH	L2	0402	chip inductor +/- 5%
3,9nH	L3	0402	chip inductor +/- 5%
Not mounted[b]	R1	0402	
22kΩ	R2	0402	+/-1%
nRF24L01+	U1	QFN20 4x4	
16MHz	X1		+/-60ppm, C_L=12pF

a. C1 and C2 must have values that match the crystals load capacitance, C_L.
b. The nRF24L01+ and nRF24L01 application example and BOM are the same with the exception of R1. R1 can be mounted for backward compatibility with nRF24L01. The use of a 1Mohm resistor externally does not have any impact on crystal performance.

Table 29. Recommended components (BOM) in nRF24L01+ with antenna matching network

11.1 PCB layout examples

Figure 33., Figure 34. and Figure 35. show a PCB layout example for the application schematic in Figure 32..

A double-sided FR-4 board of 1.6mm thickness is used. This PCB has a ground plane on the bottom layer. Additionally, there are ground areas on the component side of the board to ensure sufficient grounding of critical components. A large number of via holes connect the top layer ground areas to the bottom layer ground plane.

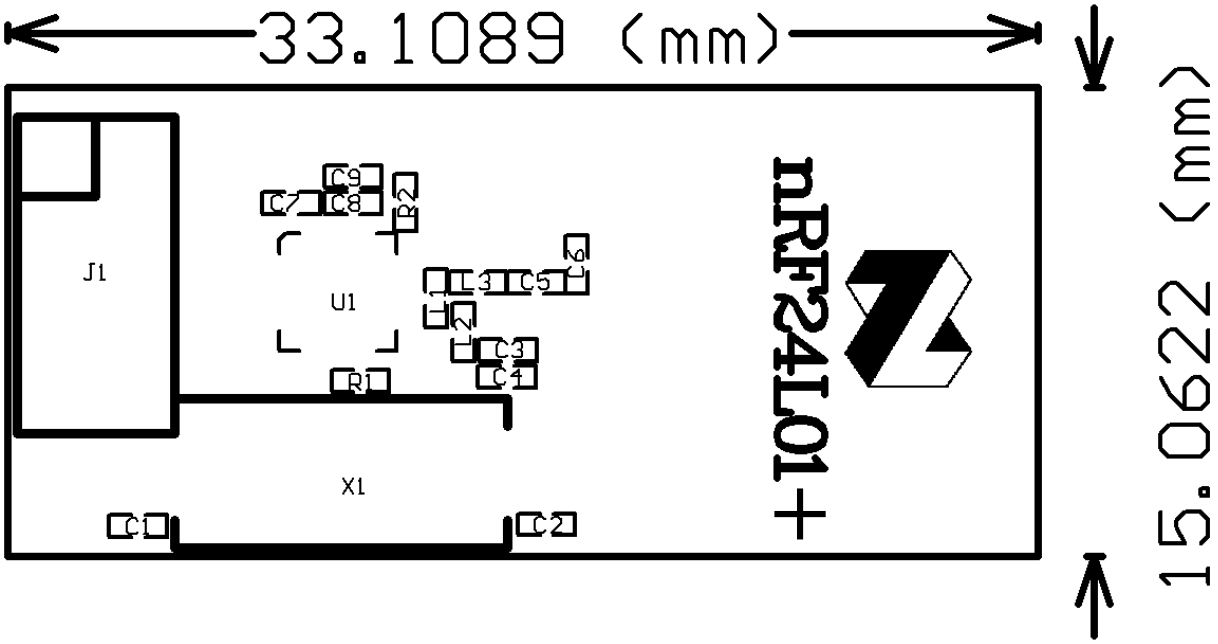


Figure 33. Top overlay (nRF24L01+ RF layout with single ended connection to PCB antenna and 0402 size passive components)

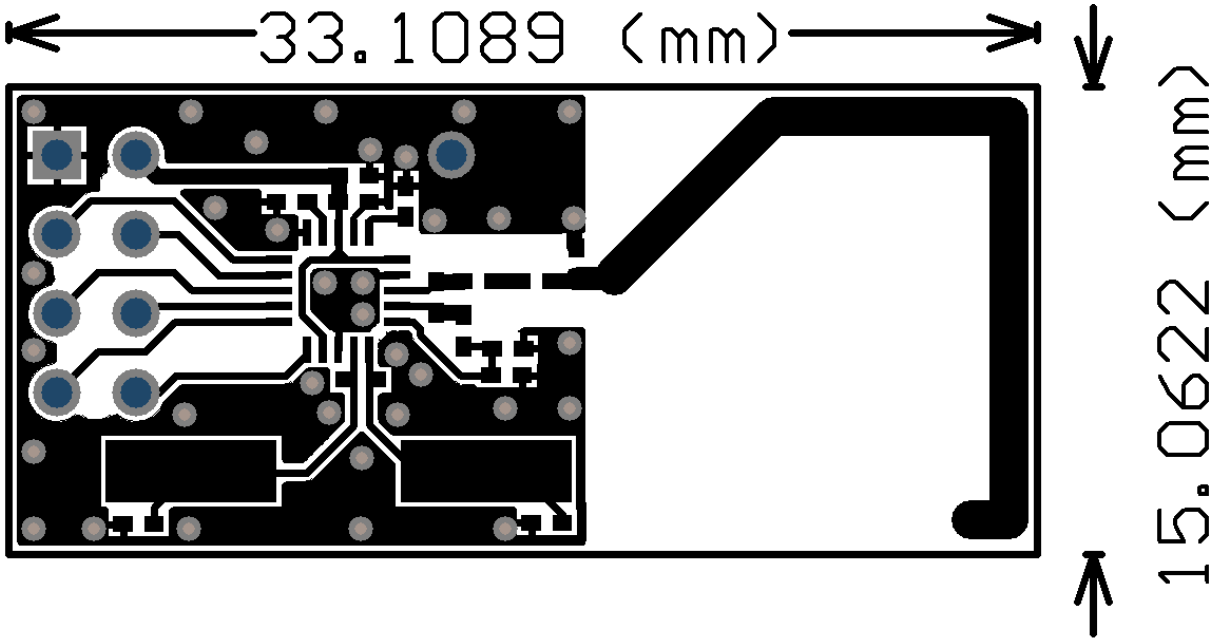


Figure 34. Top layer (nRF24L01+ RF layout with single ended connection to PCB antenna and 0402 size passive components)

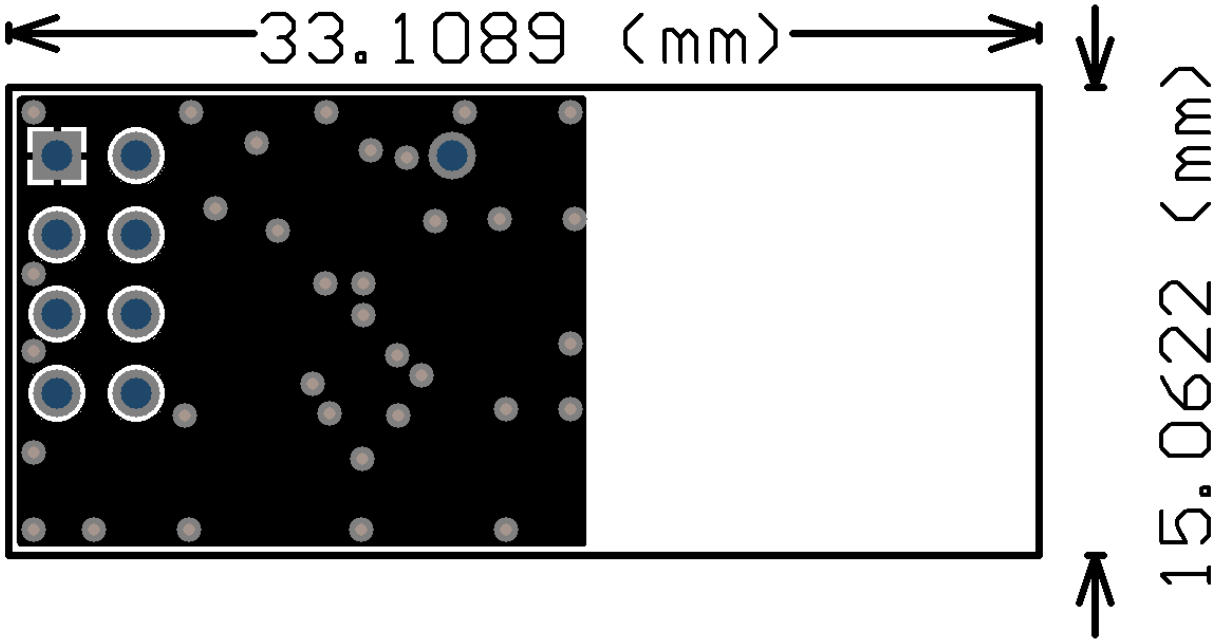


Figure 35. Bottom layer (nRF24L01+ RF layout with single ended connection to PCB antenna and 0402 size passive components

The nest figure (Figure 36., Figure 37. and Figure 38.) is for the SMA output to have a board for direct measurements at a 50Ω SMA connector.

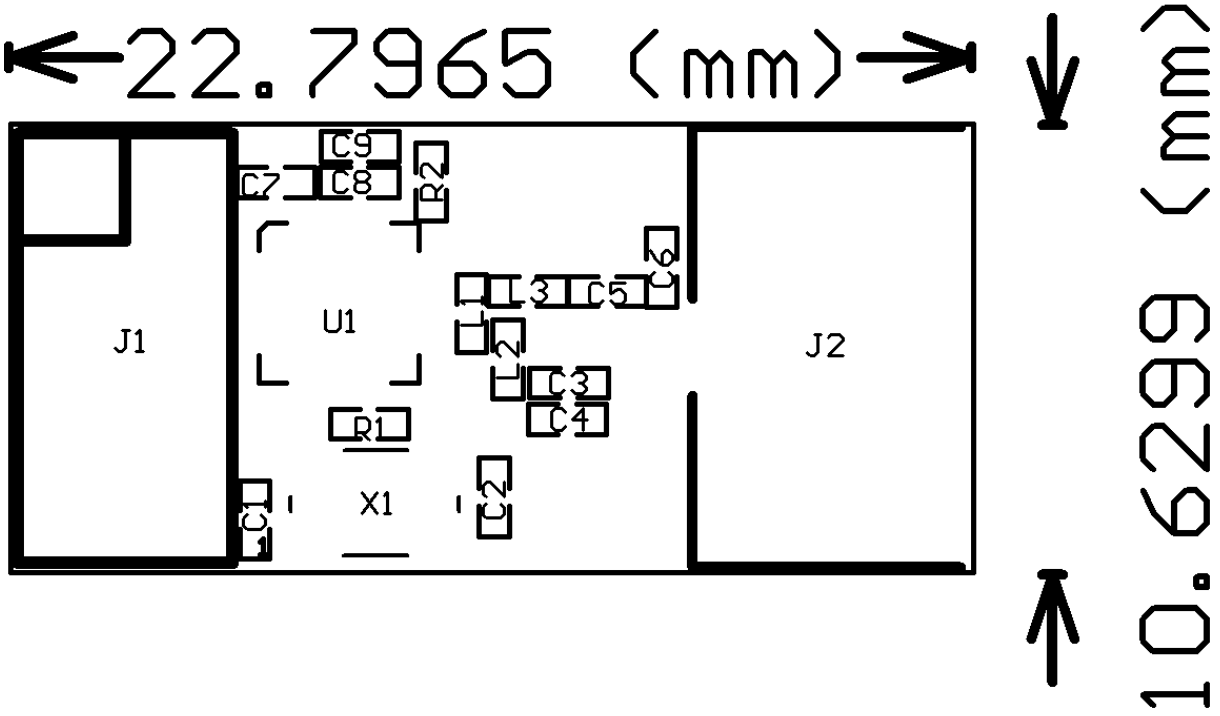


Figure 36. Top Overlay (Module with OFM crystal and SMA connector)

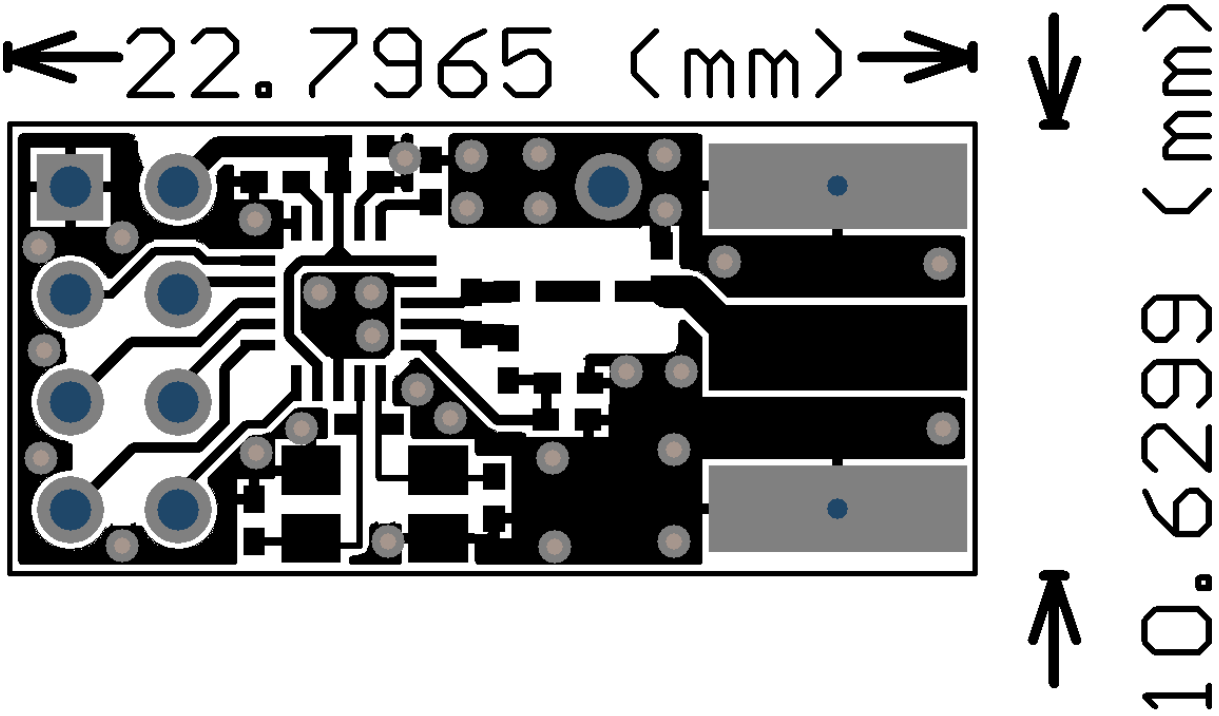


Figure 37. Top Layer (Module with OFM crystal and SMA connector)

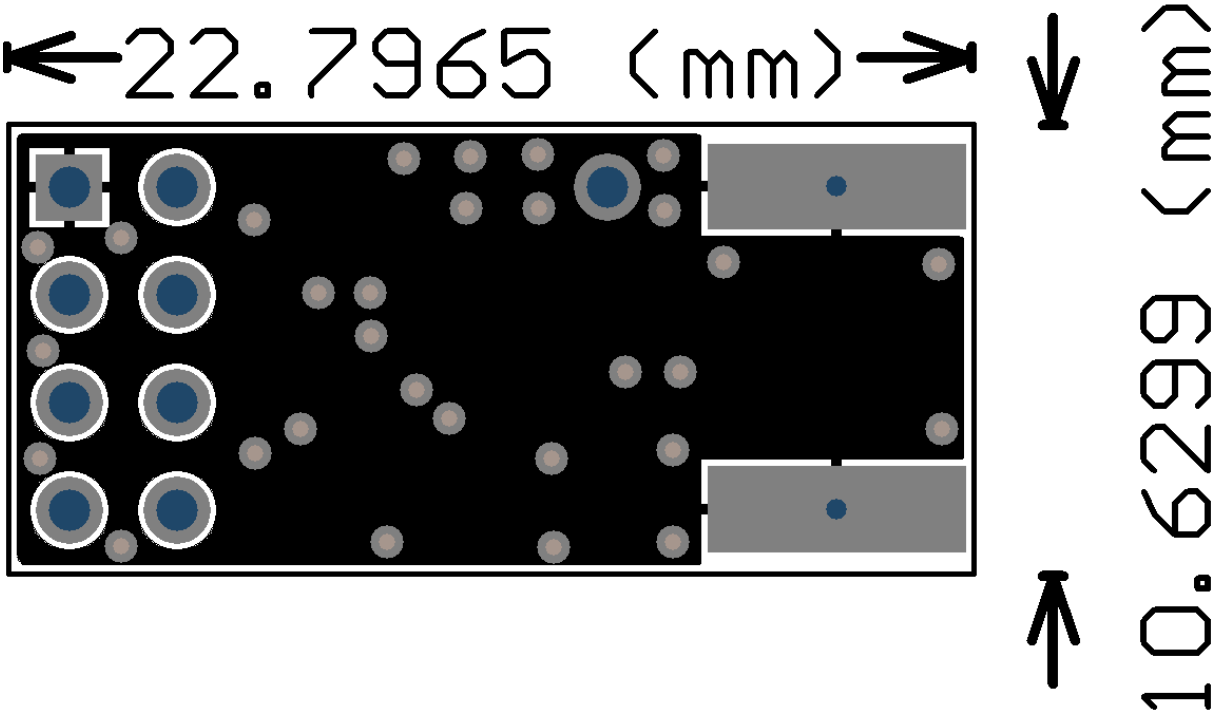
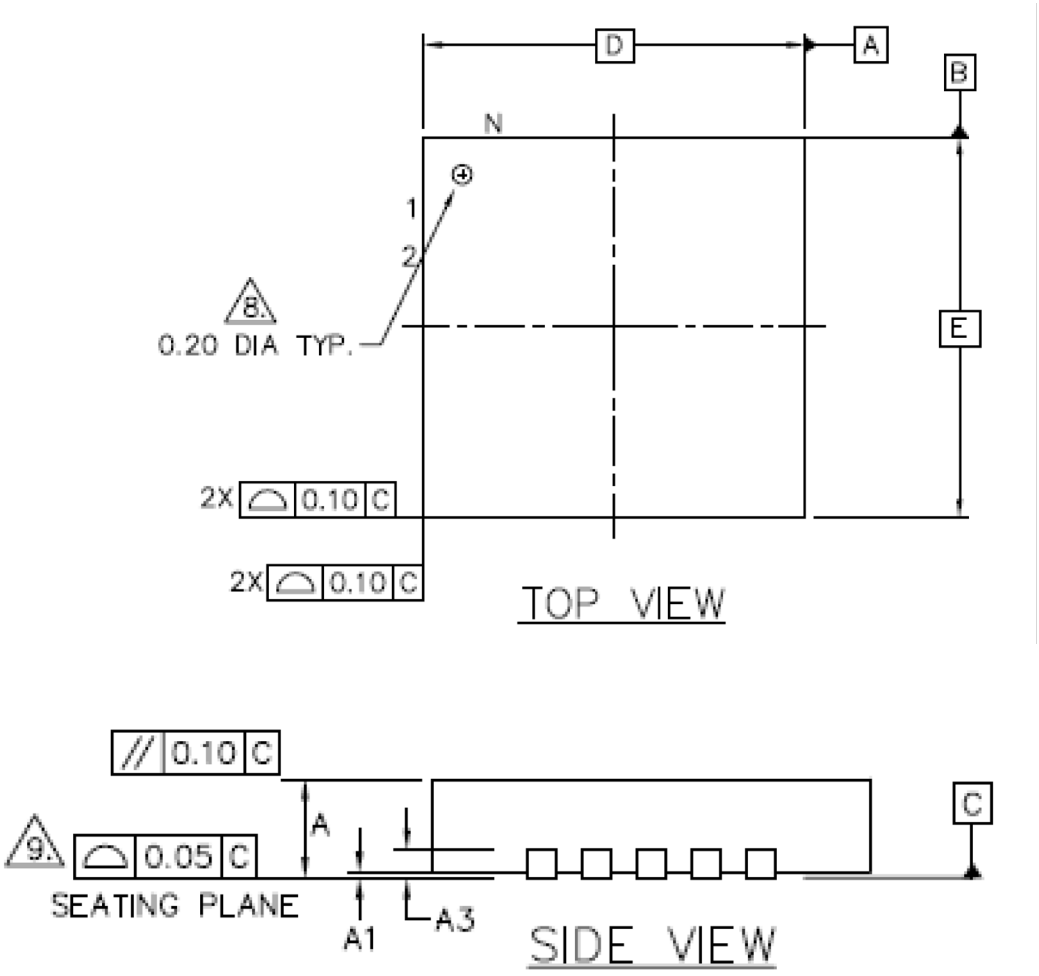
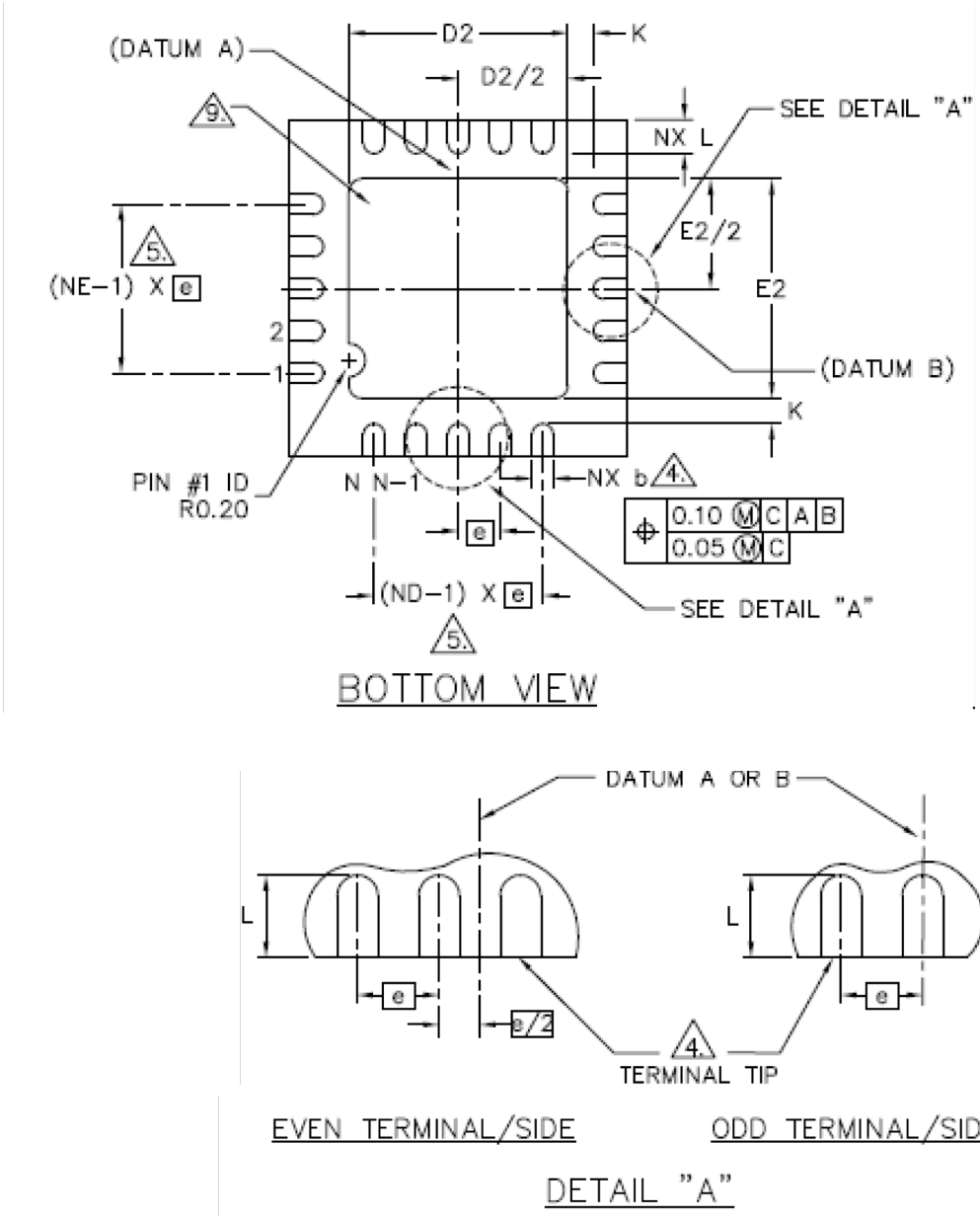


Figure 38. Bottom Layer (Module with OFM crystal and SMA connector)

12 Mechanical specifications

nRF24L01+ uses the QFN20 4x4 package, with matt tin plating.





Package Type		A	A1	A3	K	D/E	e	D2/E2	L	L1	b
Saw QFN20 (4x4 mm)	**Min.**	0.80	0.00					2.50	0.35		0.18
	Typ.	0.85	0.02	0.20	0.20	4.0	0.5 BSC	2.60	0.40	0.15	0.25
	Max	0.95	0.05	REF.	min.	BSC[a]		2.70	0.45	max	0.30

a. BSC: Basic Spacing between Centers, ref. JEDEC standard 95, page 4.17-11/A

Figure 39. nRF24L01+ Package Outline

13 Ordering information

13.1 Package marking

n	R	F		*A*	*X*
2	4	L	0	1	+
Y	*Y*	*W*	*W*	*L*	*L*

13.2 Abbreviations

Abbreviation	Definition
nRF	Fixed text
A	Variable Build Code, that is, unique code for production sites, package type and test platform
X	“X" grade, that is, Engineering Samples (optional)
YY	2 digit Year number
WW	2 digit Week number
LL	2 letter wafer lot number code

13.3 Product options

13.3.1 RF silicon

Ordering code	Package	Container	MOQ[a]
nRF24L01P-SAMPLE	4x4mm 20-pin QFN, lead free (green)	Sample box	5
nRF24L01P-T	4x4mm 20-pin QFN, lead free (green)	Tray	490
nRF24L01P-R	4x4mm 20-pin QFN, lead free (green)	Tape and reel	4000
nRF24L01P-R7	4x4mm 20-pin QFN, lead free (green)	Tape and reel	1500

a. Minimum Order Quantity

Table 30. nRF24L01+ RF silicon options

13.3.2 Development tools

Type Number	Description	Version
nRF24L01P-EVKIT	nRF24L01+ Evaluation kit	
nRF24L01P-UPGRADE	nRF24L01+ Upgrade kit for owners of nRF24L01-EVKIT	
nRF24L01P-MODULE-SMA	nRF24L01+ Evaluation kit module with SMA antenna	
nRF24L01P-MODULE-PCB	nRF24L01+ Evaluation kit module with PCB antenna	

Table 31. nRF24L01+ solution options

14 Glossary of Terms

Term	Description
ACK	Acknowledgement
ACS	Adjacent Channel Selectivity
AGC	Automatic Gain Control
ART	Auto Re-Transmit
CD	Carrier Detect
CE	Chip Enable
CLK	Clock
CRC	Cyclic Redundancy Check
CSN	Chip Select NOT
ESB	Enhanced ShockBurst™
GFSK	Gaussian Frequency Shift Keying
IM	Intermodulation
IRQ	Interrupt Request
ISM	Industrial-Scientific-Medical
LNA	Low Noise Amplifier
LSB	Least Significant Bit
LSByte	Least Significant Byte
Mbps	Megabit per second
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MSB	Most Significant Bit
MSByte	Most Significant Byte
PCB	Printed Circuit Board
PID	Packet Identity Bits
PLD	Payload
PRX	Primary RX
PTX	Primary TX
PWR_DWN	Power Down
PWR_UP	Power Up
RoHS	Restriction of use of Certain Hazardous Substances
RPD	Received Power Detector
RX	Receive
RX_DR	Receive Data Ready
SPI	Serial Peripheral Interface
TX	Transmit
TX_DS	Transmit Data Sent

Table 32. Glossary

Appendix A - Enhanced ShockBurst™ - Configuration and communication example

Enhanced ShockBurst™ transmitting payload

1. Set the configuration bit PRIM_RX low.
2. When the application MCU has data to transmit, clock the address for the receiving node (TX_ADDR) and payload data (TX_PLD) into nRF24L01+ through the SPI. The width of TX-payload is counted from the number of bytes written into the TX FIFO from the MCU. TX_PLD must be written continuously while holding **CSN** low. TX_ADDR does not have to be rewritten if it is unchanged from last transmit. If the PTX device shall receive acknowledge, configure data pipe 0 to receive the ACK packet. The RX address for data pipe 0 (RX_ADDR_P0) must be equal to the TX address (TX_ADDR) in the PTX device. For the example in Figure 14. on page 41 perform the following address settings for the TX5 device and the RX device:
   TX5 device: TX_ADDR = 0xB3B4B5B605
   TX5 device: RX_ADDR_P0 = 0xB3B4B5B605
   RX device: RX_ADDR_P5 = 0xB3B4B5B605
3. A high pulse on **CE** starts the transmission. The minimum pulse width on **CE** is 10µs.
4. nRF24L01+ ShockBurst™:
   - Radio is powered up.
   - 16MHz internal clock is started.
   - RF packet is completed (see the packet description).
   - Data is transmitted at high speed (1Mbps or 2Mbps configured by MCU).
5. If auto acknowledgement is activated (ENAA_P0=1) the radio goes into RX mode immediately, unless the NO_ACK bit is set in the received packet. If a valid packet is received in the valid acknowledgement time window, the transmission is considered a success. The TX_DS bit in the STATUS register is set high and the payload is removed from TX FIFO. If a valid ACK packet is not received in the specified time window, the payload is retransmitted (if auto retransmit is enabled). If the auto retransmit counter (ARC_CNT) exceeds the programmed maximum limit (ARC), the MAX_RT bit in the STATUS register is set high. The payload in TX FIFO is NOT removed. The **IRQ** pin is active when MAX_RT or TX_DS is high. To turn off the **IRQ** pin, reset the interrupt source by writing to the STATUS register (see Interrupt chapter). If no ACK packet is received for a packet after the maximum number of retransmits, no further packets can be transmitted before the MAX_RT interrupt is cleared. The packet loss counter (PLOS_CNT) is incremented at each MAX_RT interrupt. That is, ARC_CNT counts the number of retransmits that were required to get a single packet through. PLOS_CNT counts the number of packets that did not get through after the maximum number of retransmits.
6. nRF24L01+ goes into standby-I mode if **CE** is low. Otherwise, next payload in TX FIFO is transmitted. If TX FIFO is empty and **CE** is still high, nRF24L01+ enters standby-II mode.
7. If nRF24L01+ is in standby-II mode, it goes to standby-I mode immediately if **CE** is set low.

Enhanced ShockBurst™ receive payload

1. Select RX by setting the PRIM_RX bit in the CONFIG register to high. All data pipes that receive data must be enabled (EN_RXADDR register), enable auto acknowledgement for all pipes running Enhanced ShockBurst™ (EN_AA register), and set the correct payload widths (RX_PW_Px registers). Set up addresses as described in item 2 in the Enhanced ShockBurst™ transmitting payload example above.
2. Start Active RX mode by setting **CE** high.
3. After 130µs nRF24L01+ monitors the air for incoming communication.
4. When a valid packet is received (matching address and correct CRC), the payload is stored in the RX-FIFO, and the RX_DR bit in STATUS register is set high. The **IRQ** pin is active when RX_DR is high. RX_P_NO in STATUS register indicates what data pipe the payload has been received in.
5. If auto acknowledgement is enabled, an ACK packet is transmitted back, unless the NO_ACK bit is set in the received packet. If there is a payload in the TX_PLD FIFO, this payload is added to the ACK packet.
6. MCU sets the **CE** pin low to enter standby-I mode (low current mode).
7. MCU can clock out the payload data at a suitable rate through the SPI.
8. nRF24L01+ is now ready for entering TX or RX mode or power down mode.

Appendix B - Configuration for compatibility with nRF24XX

How to setup nRF24L01+ to receive from an nRF2401/nRF2402/nRF24E1/nRF24E2:

1. Use the same CRC configuration as the nRF2401/nRF2402/nRF24E1/nRF24E2.
2. Set the PWR_UP and PRIM_RX bit to 1.
3. Disable auto acknowledgement on the data pipe that is addressed.
4. Use the same address width as the PTX device.
5. Use the same frequency channel as the PTX device.
6. Select data rate 1Mbps or 250kbps on both nRF24L01+ and nRF2401/nRF2402/nRF24E1/nRF24E2.
7. Set correct payload width on the data pipe that is addressed.
8. Set CE high.

How to setup nRF24L01+ to transmit to an nRF2401/nRF24E1:

1. Use the same CRC configuration as the nRF2401/nRF2402/nRF24E1/nRF24E2.
2. Set the PRIM_RX bit to 0.
3. Set the Auto Retransmit Count to 0 to disable the auto retransmit functionality.
4. Use the same address width as the nRF2401/nRF2402/nRF24E1/nRF24E2.
5. Use the same frequency channel as the nRF2401/nRF2402/nRF24E1/nRF24E2.
6. Select data rate 1Mbps or 250kbps on both nRF24L01+ and nRF2401/nRF2402/nRF24E1/nRF24E2.
7. Set PWR_UP high.
8. Clock in a payload that has the same length as the nRF2401/nRF2402/nRF24E1/nRF24E2 is configured to receive.
9. Pulse CE to transmit the packet.

Appendix C - Constant carrier wave output for testing

The output power of a radio is a critical factor for achieving wanted range. Output power is also the first test criteria needed to qualify for all telecommunication regulations.

Configuration

1. Set PWR_UP = 1 and PRIM_RX = 0 in the CONFIG register.
2. Wait 1.5ms PWR_UP->standby.
3. In the RF register set:
   - CONT_WAVE = 1.
   - PLL_LOCK = 1.
   - RF_PWR.
4. Set the wanted RF channel.
5. Set **CE** high.
6. Keep **CE** high as long as the carrier is needed.

Note: Do not use REUSE_TX_PL together with CONT_WAVE=1. When both these registers are set the chip does not react when setting CE low. If however, both registers are set PWR_UP = 0 will turn TX mode off.

The nRF24L01+ should now output an unmodulated centered carrier.