

Winstar Display Co., LTD

WH4004A-YGK-CP	
	DATA:

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1. Precautions in use of LCD Modules

- (1) Avoid applying excessive shocks to the module or making any alterations or modifications to it.
- (2) Don't make extra holes on the printed circuit board, modify its shape or change the components of LCD module.
- (3) Don't disassemble the LCM.
- (4) Don't operate it above the absolute maximum rating.
- (5) Don't drop, bend or twist LCM.
- (6) Soldering: only to the I/O terminals.
- (7) Storage: please store in an anti-static container and clean environment.

2. General Specification

Item	Dimension	Unit
Number of Characters	40 characters x 4 Lines	-
Module dimension	190.0 x 54.0 x 13.6(MAX)	mm
View area	147.0 x 29.5	mm
Active area	140.45 x 23.16	mm
Dot size	0.50 x 0.55	mm
Dot pitch	0.57 x 0.62	mm
Character size	2.78 x 4.89	mm
Character pitch	3.53 x 6.09	mm
LCD type	FSTN, Negative, Transmissive, Blue	
Duty	1/16	
View direction	12 o'clock	
Backlight Type	LED White	

3. Absolute Maximum Ratings

Item	Symbol	Min	Typ	Max	Unit
Operating Temperature	T_{OP}	-20	-	+70	°C
Storage Temperature	T_{ST}	-30	-	+80	°C
Input Voltage	V_I	V_{SS}	-	V_{DD}	V
Supply Voltage For Logic	$V_{DD}-V_{SS}$	-0.3	-	6.5	V
Supply Voltage For LCD	$V_{DD}-V_0$	-0.3	-	6.5	V

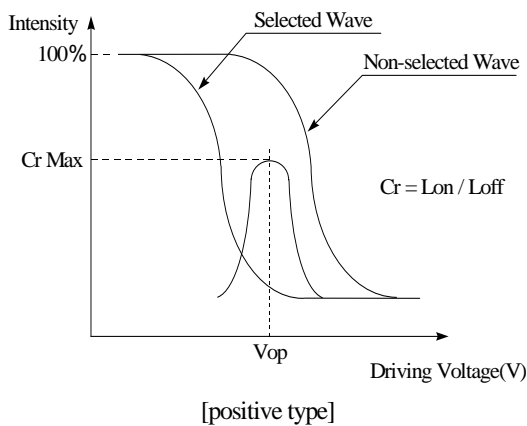
4. Electrical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage For Logic	$V_{DD}-V_{SS}$	-	4.75	-	5.25	V
Supply Voltage For LCD	$V_{DD}-V_0$	$T_a=-20^{\circ}\text{C}$	-	-	5.2	V
		$T_a=25^{\circ}\text{C}$	-	4.6	-	V
		$T_a=70^{\circ}\text{C}$	3.8	-	-	V
Input High Volt.	V_{IH}	-	2.2	-	V_{DD}	V
Input Low Volt.	V_{IL}	-	-	-	0.6	V
Output High Volt.	V_{OH}	-	2.4	-	-	V
Output Low Volt.	V_{OL}	-	-	-	0.4	V
Supply Current	I_{DD}	$V_{DD}=5\text{V}$	-	1.2	-	mA

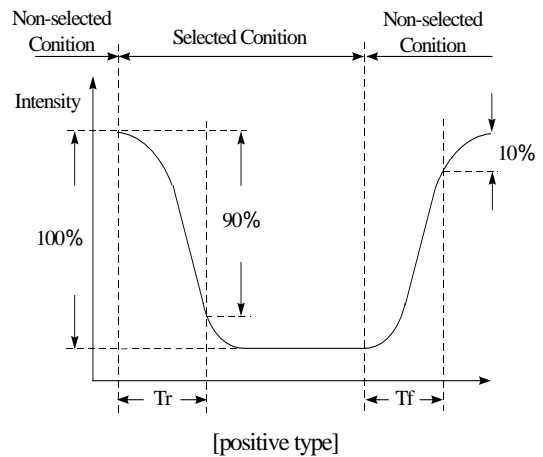
5. Optical Characteristics

Item	Symbol	Condition	Min	Typ	Max	Unit
View Angle	(V) θ	$CR \geq 2$	10	-	40	deg
	(H) φ	$CR \geq 2$	-40	-	40	deg
Contrast Ratio	CR	-	-	3	-	-
Response Time	T rise	-	-	150	200	ms
	T fall	-	-	150	200	ms

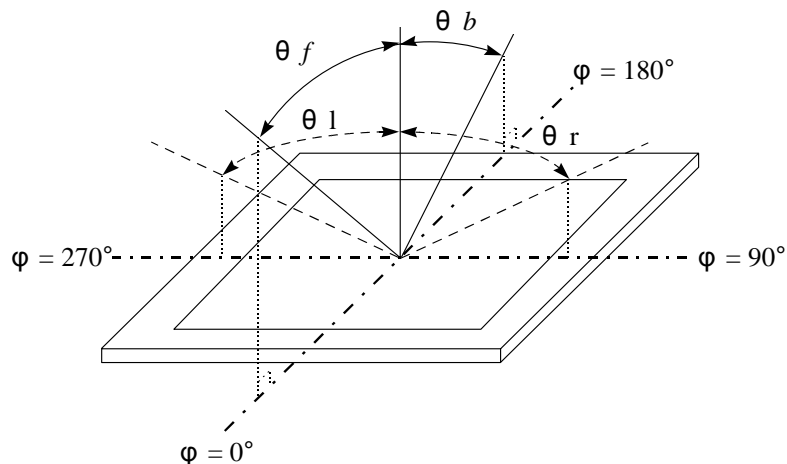
Definition of Operation Voltage (Vop)



Definition of Response Time (Tr, Tf)



Conditions : Operating Voltage : Vop Viewing Angle(θ , φ) : 0° , 0°
 Frame Frequency : 64 HZ Driving Waveform : 1/N duty , 1/a bias

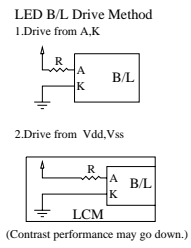
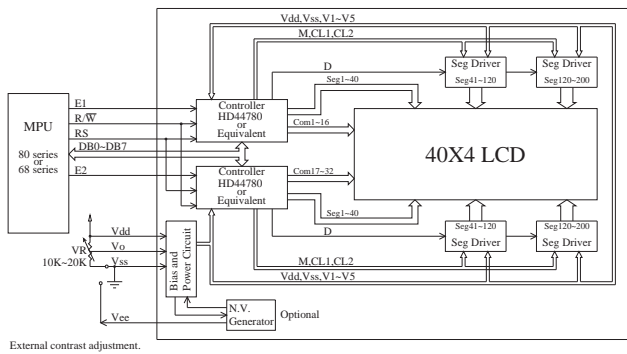
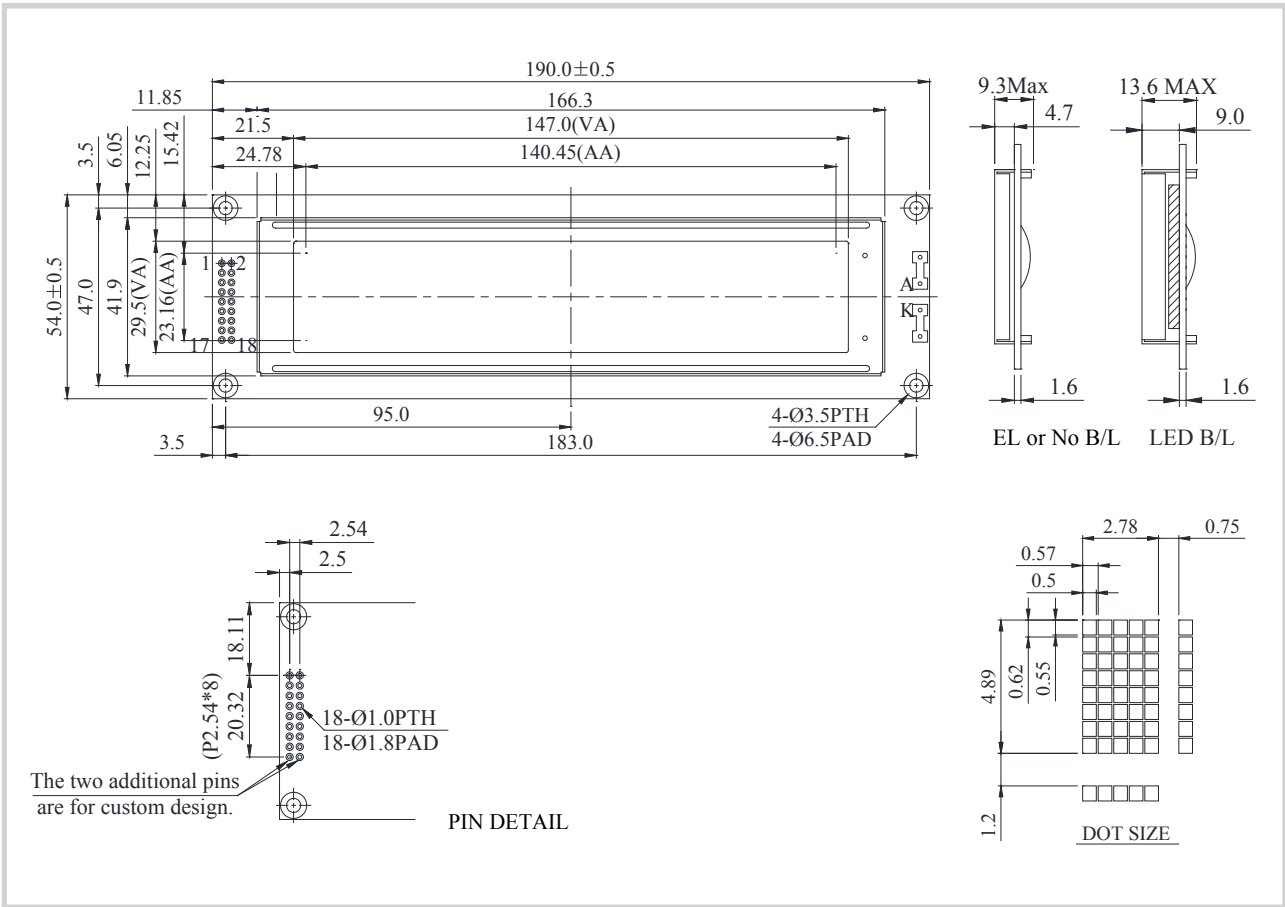


Definition of viewing angle ($CR \geq 2$)

6. Interface Pin Function

Pin No.	Symbol	Level	Description
1	DB7	H/L	Data bit 7
2	DB6	H/L	Data bit 6
3	DB5	H/L	Data bit 5
4	DB4	H/L	Data bit 4
5	DB3	H/L	Data bit 3
6	DB2	H/L	Data bit 2
7	DB1	H/L	Data bit 1
8	DB0	H/L	Data bit 0
9	E1	H,H→ L	Chip enable signal
10	W	H/L	H: Read(MPU→ Module) L: Write(MPU→ Module)
11	RS	H/L	H: DATA, L: Instruction code
12	VO	(Variable)	Operating voltage for LCD
13	ss	0V	Ground
14	DD	5.0V	Supply Voltage for logic
15	E	H,H→ L	Chip enable signal
16	NC		
17	A		LED Backlight Anode+
18	K		LED Backlight Cathode-

7. Mechanical Drawing & Block Diagram



UPPER 40X2 display

Character located	1	2	3	4	5	6	35	36	37	38	39	40
DDRAM address	00	01	02	03	04	05	22	23	24	25	26	27
DDRAM address	40	41	42	43	44	45	62	63	64	65	66	67

LOWER 40X2 display

DDRAM address	00	01	02	03	04	05	22	23	24	25	26	27
DDRAM address	40	41	42	43	44	45	62	63	64	65	66	67

E1=High
E2=High

8. Function Description

The LCD display Module is built in a LSI controller, the controller has two 8-bit registers, an instruction register (IR) and a data register (DR).

The IR stores instruction codes, such as display clear and cursor shift, and address information for display data RAM (DDRAM) and character generator (CGRAM). The IR can only be written from the MPU. The DR temporarily stores data to be written or read from DDRAM or CGRAM. When address information is written into the IR, then data is stored into the DR from DDRAM or CGRAM. By the register selector (RS) signal, these two registers can be selected.

RS	R/W	Operation
0	0	IR write as an internal operation (display clear, etc.)
0	1	Read busy flag (DB7) and address counter (DB0 to DB7)
1	0	Write data to DDRAM or CGRAM (DR to DDRAM or CGRAM)
1	1	Read data from DDRAM or CGRAM (DDRAM or CGRAM to DR)

Busy Flag (BF)

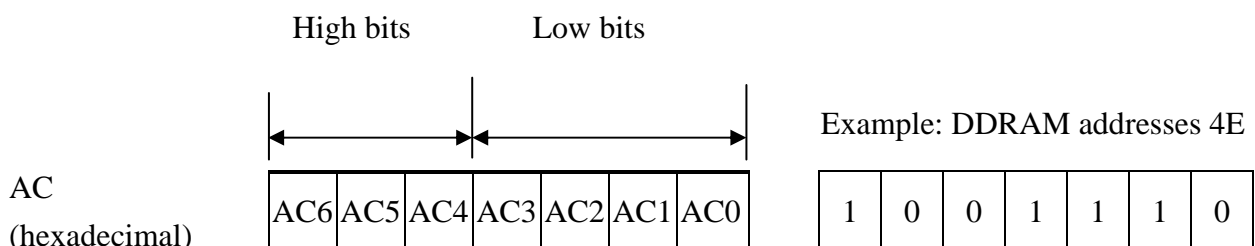
When the busy flag is 1, the controller LSI is in the internal operation mode, and the next instruction will not be accepted. When RS=0 and R/W=1, the busy flag is output to DB7. The next instruction must be written after ensuring that the busy flag is 0.

Address Counter (AC)

The address counter (AC) assigns addresses to both DDRAM and CGRAM

Display Data RAM (DDRAM)

This DDRAM is used to store the display data represented in 8-bit character codes. Its extended capacity is 80×8 bits or 80 characters. Below figure is the relationships between DDRAM



addresses and positions on the liquid crystal display.

Display position DDRAM address

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

2-Line by 16-Character Display

Character Generator ROM (CGROM)

The CGROM generate 5×8 dot or 5×10 dot character patterns from 8-bit character codes. See Table 2.

Character Generator RAM (CGRAM)

In CGRAM, the user can rewrite character by program. For 5×8 dots, eight character patterns can be written, and for 5×10 dots, four character patterns can be written.

Write into DDRAM the character code at the addresses shown as the left column of table 1. To show the character patterns stored in CGRAM.

Relationship between CGRAM Addresses, Character Codes (DDRAM) and Character patterns

Table1.

For 5 * 8 dot character patterns

Character Codes (DDRAM data)								CGRAM Address								Character Patterns (CGRAM data)													
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
High				Low				High				Low				High				Low									
0 0 0 0 * 0 0 0								0 0 0								0 0 0	* * *								0	Character pattern (1)			
																0 0 1	* * *								0 0 0				
																0 1 0	* * *								0 0 0				
																0 1 1	* * *								0				
																1 0 0	* * *								0				
																1 0 1	* * *								0 0 0				
																1 1 0	* * *								0 0 0				
																1 1 1	* * *								0 0 0 0 0 0				
																0 0 0	* * *								0 0 0 0				
																0 0 1	* * *								0 0 0 0				
0 0 0 0 * 0 0 1								0 0 1								0 1 1	* * *								0 0	Character pattern (2)			
																1 0 0	* * *								0 0 0 0 0 0				
																1 0 1	* * *								0 0 0 0 0 0				
																1 1 0	* * *								0 0 0 0 0 0				
																1 1 1	* * *								0 0 0 0 0 0				
																0 0 0	* * *								0 0 0 0 0 0				
																0 1 0	* * *								0 0 0 0 0 0				
																0 1 1	* * *								0 0 0 0 0 0				
																1 0 0	* * *								0 0 0 0 0 0				
																1 0 1	* * *								0 0 0 0 0 0				
0 0 0 0 * 1 1 1								1 1 1								1 0 0	* * *								0	Cursor pattern			
																1 0 1	* * *												
																1 1 0	* * *												
																1 1 1	* * *												

For 5 * 10 dot character patterns

Character Codes (DDRAM data)										CGRAM Address										Character Patterns (CGRAM data)												
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0			
High					Low					High					Low					High					Low							
0 0 0 0 * 0 0 0										0 0										0 0 0 0 0	* * *										0	Character pattern
																				0 0 0 0 1	* * *										0 0 0 0 0 0	
																				0 0 1 0	* * *										0 0 0 0 0	
																				0 0 1 1	* * *										0 0 0	
																				0 1 0 0	* * *										0 0 0 0	
																				0 1 0 1	* * *										0 0 0 0	
																				0 1 1 0	* * *										0 0 0 0	
																				0 1 1 1	* * *										0 0 0 0 0 0	
																				1 0 0 0	* * *										0 0 0 0 0 0	
																				1 0 0 1	* * *										0 0 0 0 0 0	
0 0 0 0 * 1 1 1										1 1 1 1										1 0 1 0	* * *										0	Cursor pattern
																				1 0 1 1	* * *											
																				1 1 0 0	* * *											
																				1 1 0 1	* * *											

■ : " High "

9. Character Generator ROM Pattern

Table.2

Upper 4 bit Lower 4 bit	LLLL	LLLH	LLHL	LLHH	LHLL	LHLH	LHHL	LHHH	HLLL	HLLH	HLHL	HLHH	HHLL	HHLH	HHHL	HHHH
LLLL	CG RAM (1)			0	1	2	3	4			5	6	7	8	9	*
LLLH	CG RAM (2)	!	"	#	\$	%	&	'			()	*	+	,	-
LLHL	CG RAM (3)	.	:	;	<	=	>	?@			[]	^	_	~	0
LLHH	CG RAM (4)	1	2	3	4	5	6	7			8	9	*	+	,	-
LHLL	CG RAM (5)	.	:	;	<	=	>	?@			[]	^	_	~	0
LHLH	CG RAM (6)	!	"	#	\$	%	&	'			()	*	+	,	-
LHHL	CG RAM (7)	.	:	;	<	=	>	?@			[]	^	_	~	0
LHHH	CG RAM (8)	1	2	3	4	5	6	7			8	9	*	+	,	-
HLLL	CG RAM (1)	.	:	;	<	=	>	?@			[]	^	_	~	0
HLLH	CG RAM (2)	!	"	#	\$	%	&	'			()	*	+	,	-
HLHL	CG RAM (3)	.	:	;	<	=	>	?@			[]	^	_	~	0
HLHH	CG RAM (4)	1	2	3	4	5	6	7			8	9	*	+	,	-
HHLL	CG RAM (5)	.	:	;	<	=	>	?@			[]	^	_	~	0
HHLH	CG RAM (6)	!	"	#	\$	%	&	'			()	*	+	,	-
HHHL	CG RAM (7)	.	:	;	<	=	>	?@			[]	^	_	~	0
HHHH	CG RAM (8)	1	2	3	4	5	6	7			8	9	*	+	,	-

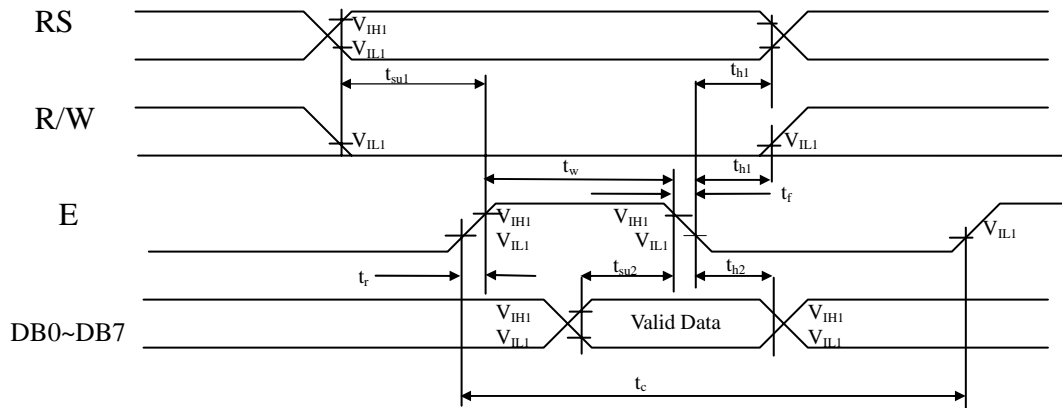
10. Instruction Table

Instruction	Instruction Code										Description	Execution time (fosc=270Khz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "00H" to DDRAM and set DDRAM address to "00H" from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and enable the shift of entire display.	39μ s
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and blinking of cursor (B) on/off control bit.	39μ s
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	39μ s
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL:8-bit/4-bit), numbers of display line (N:2-line/1-line)and, display font type (F:5×11 dots/5×8 dots)	39μ s
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39μ s
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39μ s
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0μ s
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43μ s
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43μ s

* " - " : don't care

11. Timing Characteristics

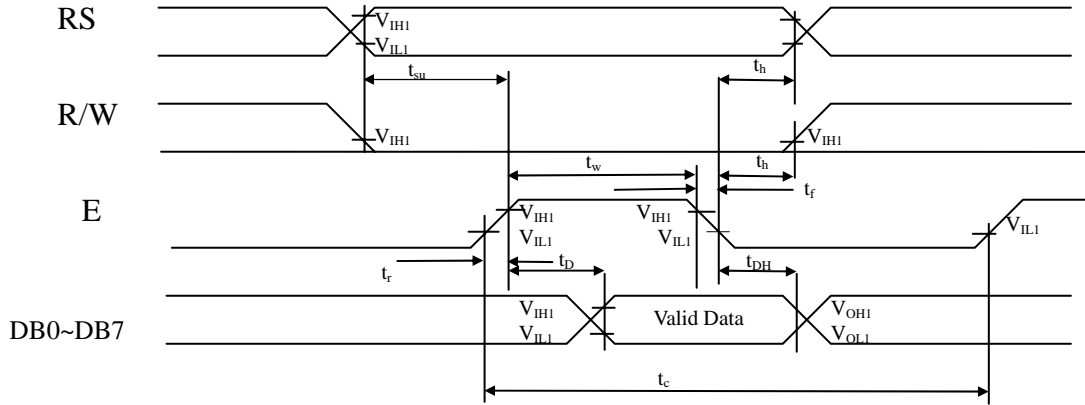
12.1 Write Operation



($V_{DD}=4.5V\sim 5.5V$, $T_a=-30\sim +85^{\circ}C$)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Write Mode	E cycle Time	t_c	500	-	-	ns
	E Rise/Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	t_w	230	-	-	
	R/W and RS Setup Time	t_{su1}	40	-	-	
	R/W and RS Hold Time	t_{h1}	10	-	-	
	Data Setup Time	t_{su2}	80	-	-	
	Data Hold Time	t_{h2}	10	-	-	

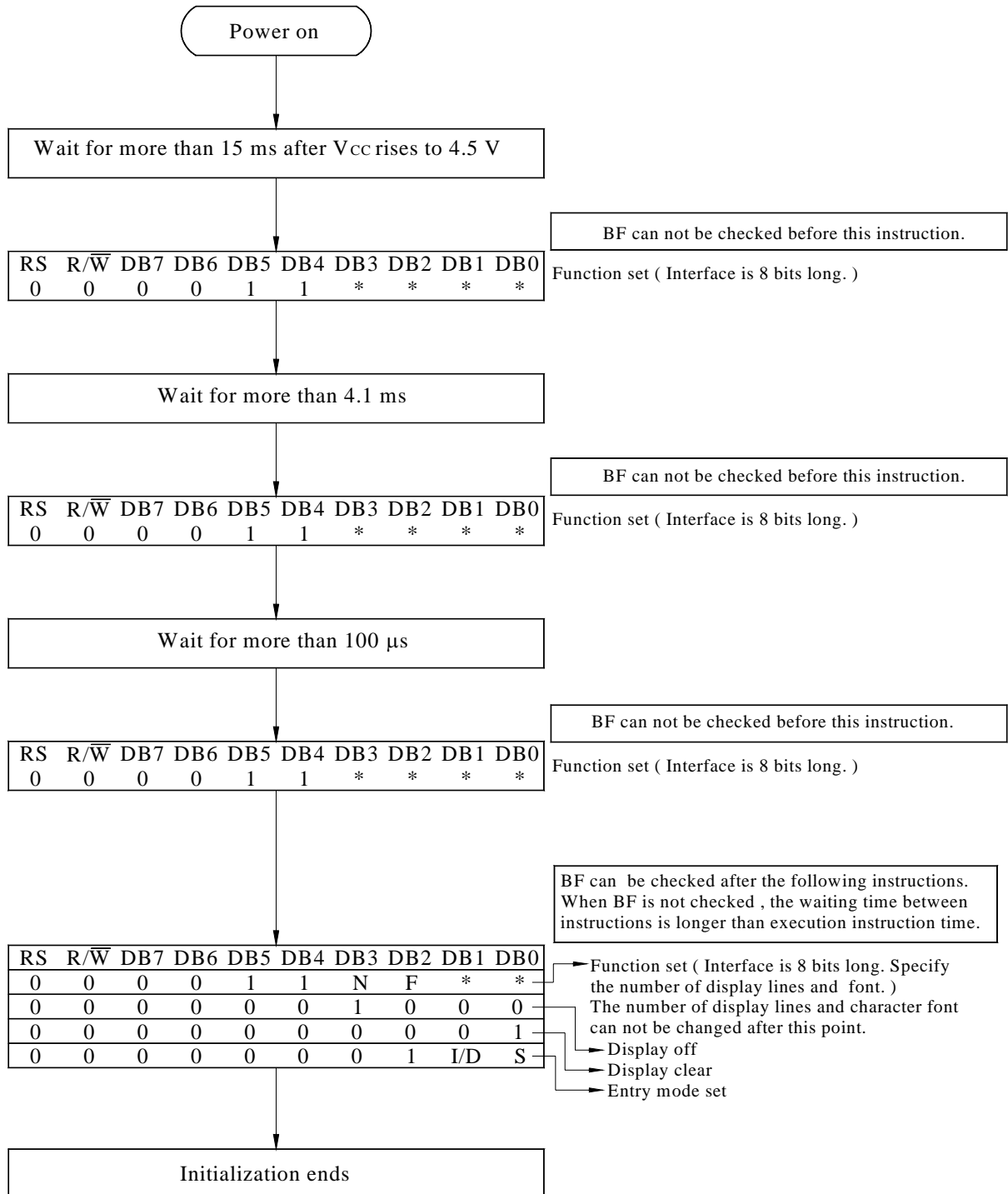
12.2 Read Operation



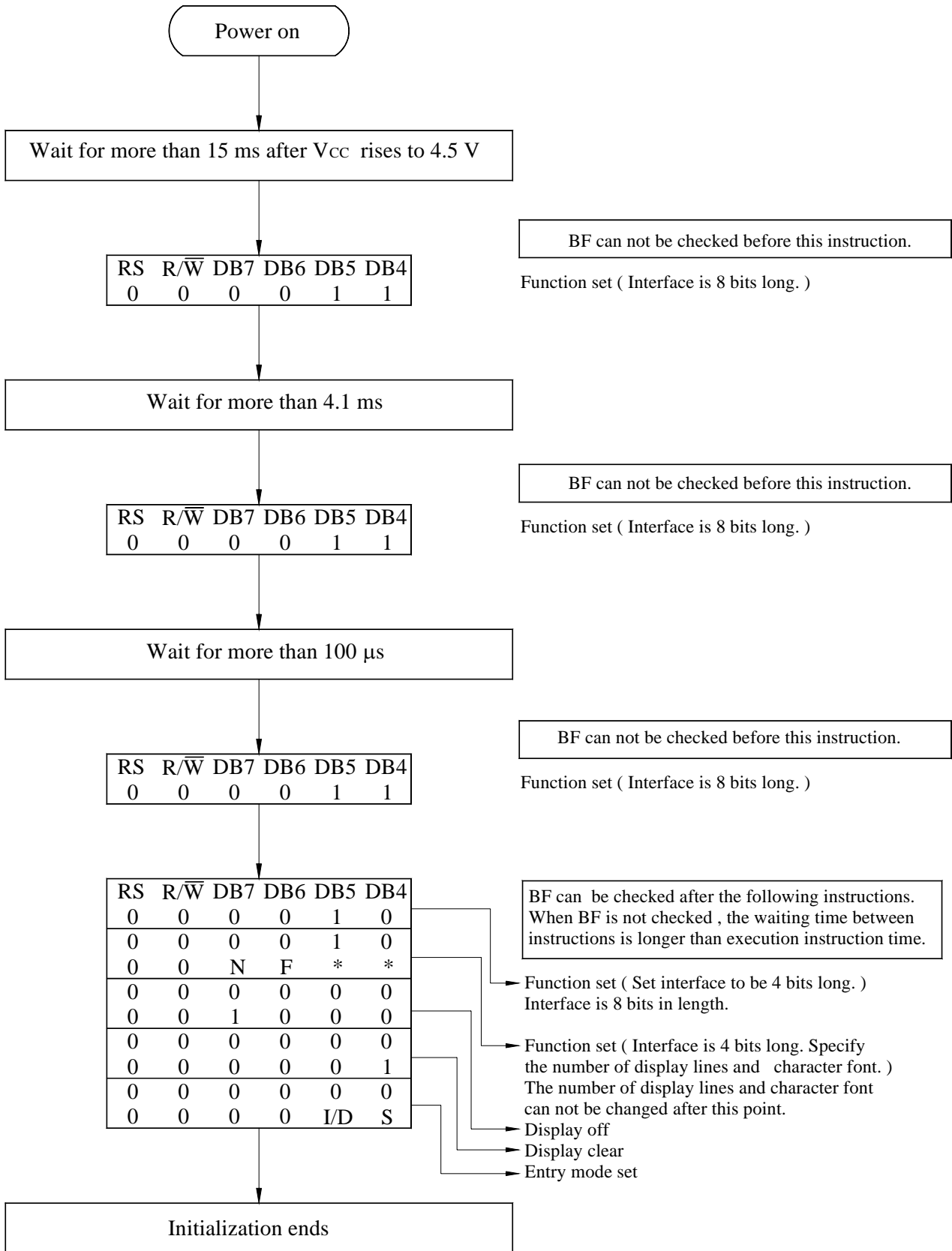
($V_{DD}=4.5V\sim 5.5V$, $T_a=-30\sim +85^{\circ}C$)

Mode	Characteristic	Symbol	Min.	Typ.	Max.	Unit
Read Mode	E cycle Time	t_c	500	-	-	ns
	E Rise/Fall Time	t_R, t_F	-	-	20	
	E Pulse Width (High, Low)	t_w	230	-	-	
	R/W and RS Setup Time	t_{su}	40	-	-	
	R/W and RS Hold Time	t_h	10	-	-	
	Data Output Delay Time	t_D	-	-	120	
	Data Hold Time	t_{DH}	5	-	-	

13. Initializing of LCM **8Bit Interface**



13. Initializing of LCM **4Bit Interface**



16. Backlight Information

Specification

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	TEST CONDITION
Supply Current	I _{LED}	—	150	200	mA	V=5V
Supply Voltage	V	-	4.2	5.5	V	-
Reverse Voltage	V _R	-	-	8	V	-
Life Time	-	-	100000	-	Hr.	V ≤ 5V
Color	White					