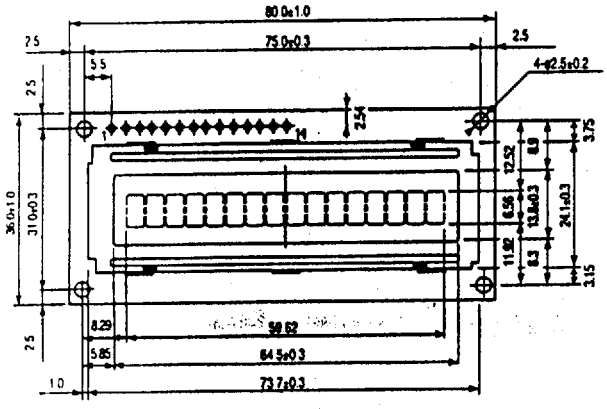
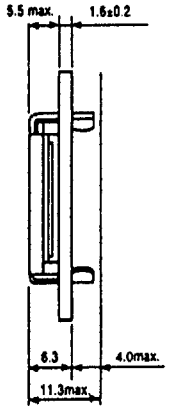
SPEC. SHEET
FOR
8944-OP

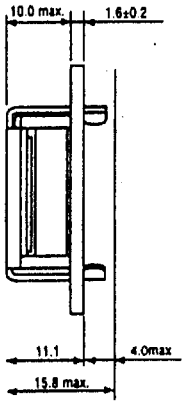
(1x16) Unit: mm General Tolerance ±0.5 mm

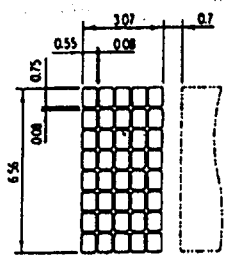


Reflective/EL Backlight



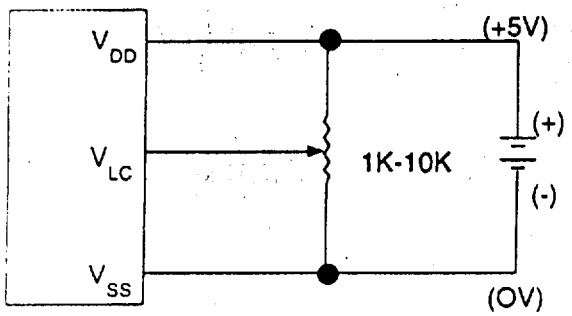
LED Backlight





Pin Functions		
No.	Name	Function
1	V_{SS}	GND
2	V_{DD}	Power supply voltage + 5 V
3	V_{LC}	Liquid crystal driving voltage
4	RS	L: Instruction code input, H: Data input
5	R/W	L: Data write from MPU to LCM, H: Data read from LCM to MPU
6	E	Enable
7	DB0	Data bus line
8	DB1	Data bus line
9	DB2	Data bus line
10	DB3	Data bus line
11	DB4	Data bus line
12	DB5	Data bus line
13	DB6	Data bus line
14	DB7	Data bus line

Standard STN



- The above schematic applies to all standard temperature supertwist character modules A variable or fixed resistor must be used on any LCD module as it appears in the above schematic.
- A variable resistor is advisable, especially for stationary equipment. The variable resistor allows the user to adjust the voltage, to get maximum contrast in relationship to whatever angle the user is viewing the LCD (within the optimum viewing range). A variable also allows the user to adjust the voltage for any temperature fluctuations between 0° and 50°C.
- A fixed resistor limits the LCD to a finite voltage and therefore a very limited viewing angle. Fixed resistors should be used in those applications where the display can be adjusted to the particular user (i.e., hand-held products).

READ TIMING CHARACTERISTICS

V_{DD}=5.0V±5%, V_{SS}=0V, T=0°C to 50°C

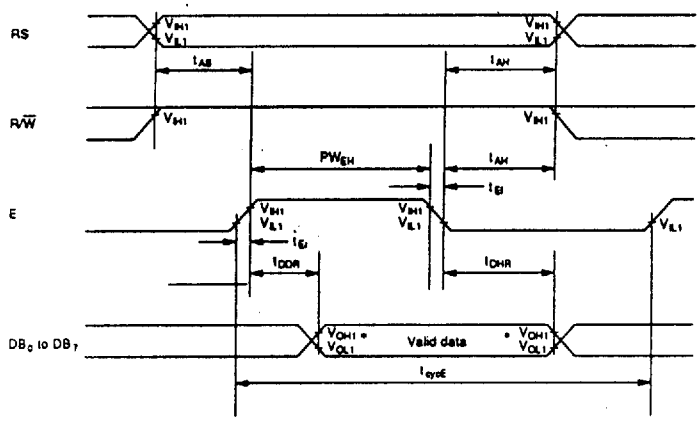
Item	Symbol	Standard		Unit
		Min.	Max.	
Enable cycle time	$t_{CYC}E$	500	—	ns
Enable pulse width High Level	PW_{EH}	230	—	ns
Enable rise and fall time	t_{ER}, t_{EF}	—	20	ns
Setup time RS,R/W—E	t_{AS}	140	—	ns
Address hold time	t_{AH}	10	—	ns
Data delay time	t_{DDR}	—	160	ns
Data hold time	t_H	5	—	ns

WRITE TIMING CHARACTERISTICS

V_{DD}=5.0V±5%, V_{SS}=0V, T=0°C to 50°C

Item	Symbol	Standard		Unit
		Min.	Max.	
Enable cycle time	$t_{CYC}E$	500	—	ns
Enable pulse width High Level	PW_{EH}	230	—	ns
Enable rise and fall time	t_{ER}, t_{EF}	—	20	ns
Setup time RS,R/W—E	t_{AS}	140	—	ns
Address hold time	t_{AH}	10	—	ns
Data delay time	t_{DDR}	80	—	ns
Data hold time	t_H	10	—	ns

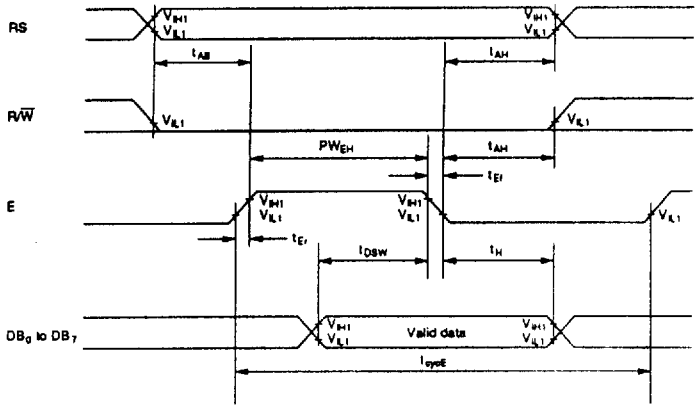
READ OPERATION



Note: * VOL1 is assumed to be 0.8 V at 2 MHz operation.

DATA READ FROM MODULE TO MPU

WRITE OPERATION



DATA WRITE FROM MPU TO MODULE

INSTRUCTION CODES

Instruction	Set	Instruction Code								Description	Execution Time (when f_{cp} or f_{osc} is 250 kHz)
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display memory and returns the cursor to the home position (Address 0).	82 μs ~ 1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0) shifted to the original position. DD RAM contents remain unchanged.	40 μs ~ 1.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies to or not to shift the display. These operations write and read.	40 μs ~ 1.64ms
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	(D) is display ON/OFF control; memory remains unchanged in OFF condition. (C) cursor ON/OFF (B) blinking cursor.	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font (F).	40 μs
Set CG RAM Address	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μs
Write Data to CG or to DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs

* Doesn't matter

DD RAM: Display data RAM
CG RAM: Character generator RAM
A_{CG}: CG RAM address
A_{DD}: DD RAM address corresponds to cursor address
A_C: Address counter used for both DD RAM and CG RAM address

I/D = 1: Increment
I/D = 0: Decrement

S = 1: Display shift
S = 0: No display shift

D = 1: Display ON
D = 0: Display OFF

C = 1: Cursor ON
C = 0: Cursor OFF

B = 1: Blink ON
B = 0: Blink OFF

S/C = 1: Display shift
S/C = 0: Cursor movement

BF = 1: Internal operation in progress
BF = 0: Instruction can be accepted

R/L = 1: Right shift
R/L = 0: Left shift

DL = 1: 8 bits
DL = 0: 4 bits

N = 1: 2 lines (L1671)

F = 0: 5 x 7 dot matrix

Execution times in the above table indicate the minimum values when operating frequency is 250 kHz.

When f_{osc} is 270 kHz: 40μs x 250/250 = 37μs

CHARACTER FONT CODES (5 x 7 DOT MATRIX)

Upper 4 Bit Hexadecimal

Lower 4 Bit Hexadecimal

Lower 4 bits \ Upper 4 bits	0000 (0)	0010 (2)	0011 (3)	0100 (4)	0101 (5)	0110 (6)	0111 (7)	1010 (A)	1011 (B)	1100 (C)	1101 (D)	1110 (E)	1111 (F)
××××0000 (0)	CG RAM (1)												
××××0001 (1)	(2)												
××××0010 (2)	(3)												
××××0011 (3)	(4)												
××××0100 (4)	(5)												
××××0101 (5)	(6)												
××××0110 (6)	(7)												
××××0111 (7)	(8)												
××××1000 (8)	(1)												
××××1001 (9)	(2)												
××××1010 (A)	(3)												
××××1011 (B)	(4)												
××××1100 (C)	(5)												
××××1101 (D)	(6)												
××××1110 (E)	(7)												
××××1111 (F)	(8)												