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**SPECIFICATION  
FOR  
LCM MODULE**

**MODULE NO.: LCM4004A-Y**

**REVISION NO.:     A**

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Customer Approval:

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	SIGNATURE
PREPARED BY	
VERIFIED BY	
APPROVED BY	

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### 1.3 Absolute Maximum Ratings

Item	Symbol	Condition	Min.	Max.	Unit
System Power Supply Voltage	VDD	-	-0.3	5.5	V
LCD Driver Supply Voltage	VLCD	-	VDD-12	VDD-0.3	V
Input Voltage	V <sub>IN</sub>	-	-0.3	VDD + 0.3	V
Operating Temperature	T <sub>OP</sub>	-	-10	60	°C
Storage Temperature	T <sub>ST</sub>	-	-20	70	°C
Storage Humidity	H <sub>D</sub>	Ta < 40 °C	20	90	%RH

### 1.4 DC Electrical Characteristics

VDD = 5.0V ± 0.2V, GND = 0V, Ta = 25°C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Logic Supply Voltage	VDD	-	3.0	5.0	5.5	V
Input High Voltage	V <sub>IH</sub>	-	0.8VDD	-	VDD	V
Input Low Voltage	V <sub>IL</sub>	-	GND	-	0.3VDD	V
Output High Voltage	V <sub>OH</sub>	-	0.7VDD	-	VDD	V
Output Low Voltage	V <sub>OL</sub>	-	GND	-	0.2VDD	V

### 1.5 Backlight Characteristics

LCD Module without LED Backlight

Electrical / Optical Characteristics

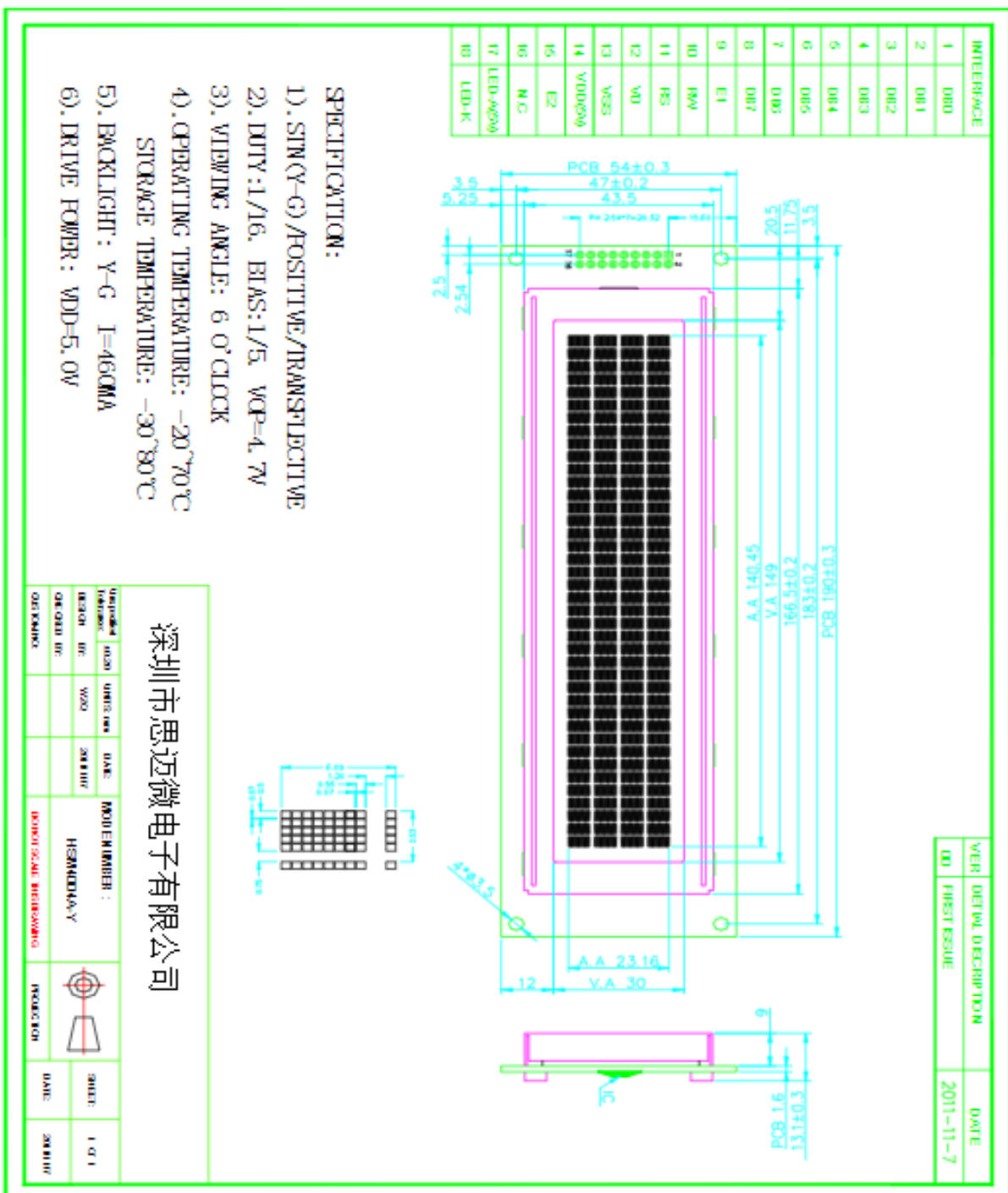
Ta = 25°C

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Forward Voltage	V <sub>f</sub>	I <sub>f</sub> =460mA	4.1	4.2	4.4	V
Reverse Current	I <sub>r</sub>	I <sub>f</sub> =8v			--	uA
Average Brightness	I <sub>V</sub>	I <sub>f</sub> =460mA				cd/m <sup>2</sup>
Wavelength (Without LCD)	λ <sub>d</sub>	I <sub>f</sub> =460mA	--	--	--	nm
Luminous Intensity (without LCD)	L <sub>v</sub> Sub	I <sub>f</sub> =460mA				cd/m <sup>2</sup>
Uniformity	Δ%	I <sub>v</sub> Min / I <sub>v</sub> Max *100%	--	-	-	%
Color	Y-G					

## 2. MODULE STRUCTURE

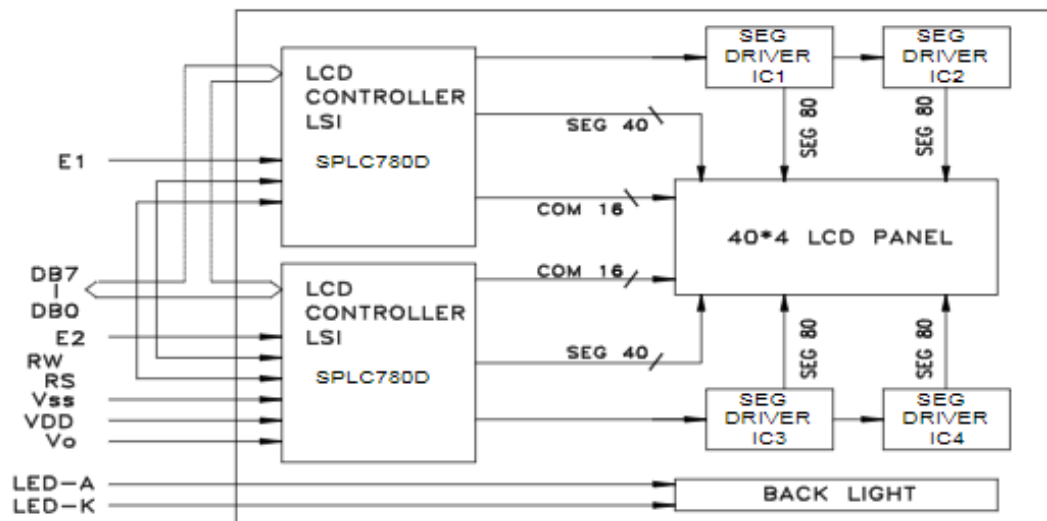
### 2.1 Counter Drawing

#### 2.1.1 LCM Mechanical Diagram



## 2.2 Interface Pin Description

No.	Symbol	Function
1--8	DB0—DB7	Data Bus
9	E1	Enable Signal U4 (TOP)
10	R/W	Read/Write Select
11	RS	Data/Instruction Select
12	VO	Contrast Adjustment
13	VSS	Ground (0V)
14	VDD	Supply Voltage for Logic (+5.0V)
15	E2	Enable Signal U1 (BOTTOM)
16	N.C	-----
17	LED_A	LED Power Supply + (5.0V)
18	LED_K	LED Power Supply - (0V)



Character located	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
E1 DDRAMaddress	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
E1 DDRAMaddress	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67
Character located	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
E2 DDRAMaddress	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	20	21	22	23	24	25	26	27
E2 DDRAMaddress	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F	50	51	52	53	54	55	56	57	58	59	5A	5B	5C	5D	5E	5F	60	61	62	63	64	65	66	67

## 2.3 Timing Characteristics

### DC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Current	I <sub>DD</sub>	-	0.55	0.8	mA	External clock (Note)
Input High Voltage	V <sub>IH1</sub>	2.2	-	VDD	V	Pins:(E, RS, R/W, DB7 - 0)
Input Low Voltage	V <sub>IL1</sub>	-0.3	-	0.6	V	
Input High Voltage	V <sub>IH2</sub>	VDD-1	-	VDD	V	Pin OSC1
Input Low Voltage	V <sub>IL2</sub>	-0.2	-	1.0	V	Pin OSC1
Input High Current	I <sub>IH</sub>	-2.0	-	2.0	μA	Pins: (RS, R/W, DB7 - 0)
Input Low Current	I <sub>IL</sub>	-20.0	-50.0	-100.0	μA	VDD = 5.0V
Output High Voltage (TTL)	V <sub>OH1</sub>	2.4	-	VDD	V	I <sub>OH</sub> = -0.1mA Pins: DB7 - 0
Output Low Voltage (TTL)	V <sub>OL1</sub>	-	-	0.4	V	I <sub>OL</sub> = 0.1mA Pins: DB7 - 0
Output High Voltage (CMOS)	V <sub>OH2</sub>	0.9VDD	-	VDD	V	I <sub>OH</sub> = -40.0μA, Pins: CL1, CL2, M, D
Output Low Voltage (CMOS)	V <sub>OL2</sub>	-	-	0.1VDD	V	I <sub>OL</sub> = 40.0μA, Pins: CL1, CL2, M, D
Driver ON Resistance (COM)	R <sub>COM</sub>	-	-	20.0	KΩ	I <sub>D</sub> = ±50.0μA, V <sub>LCD</sub> = 4.0V Pins: COM16 - 1
Driver ON Resistance (SEG)	R <sub>SEG</sub>	-	-	30.0	KΩ	I <sub>D</sub> = ±50.0μA, V <sub>LCD</sub> = 4.0V Pins: SEG40 - 1
LCD Voltage	V <sub>LCD</sub>	3.0	-	11.0	V	VDD - V5, 1/4 bias or 1/5 bias

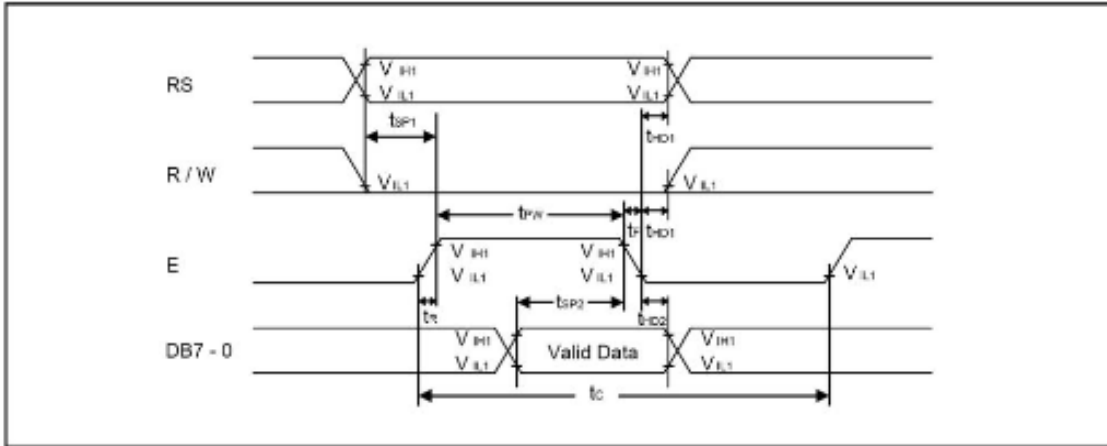
Note: F<sub>OSC</sub> = 250.0KHz, VDD = 5.0V, pin E = 'L', RS, R/W, DB7 - 0 are open, all outputs are no loads.

### AC Characteristics

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
OSC Frequency	F <sub>OSC1</sub>	190.0	270.0	350.0	KHz	VDD = 5.0V Rf = 91.0KΩ±2%

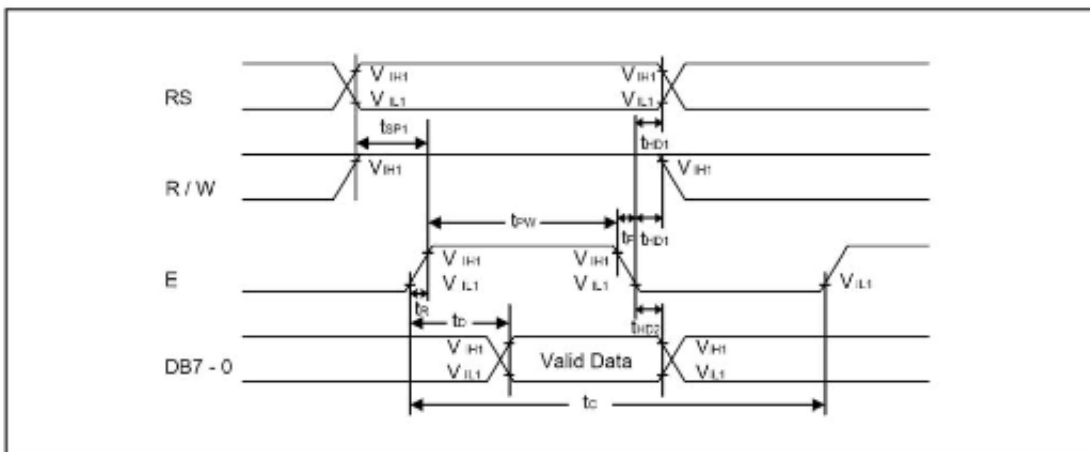
## Timing Diagram

### Writing mode



Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	$t_c$	400.0	-	-	ns	Pin E
E Pulse Width	$t_w$	150.0	-	-	ns	Pin E
E Rise/Fall Time	$t_r, t_f$	-	-	25.0	ns	Pin E
Address Setup Time	$t_{SP1}$	30.0	-	-	ns	Pins: RS, R/W, E
Address Hold Time	$t_{HD1}$	10.0	-	-	ns	Pins: RS, R/W, E
Data Setup Time	$t_{SP2}$	40.0	-	-	ns	Pins: DB7 - 0
Data Hold Time	$t_{HD2}$	10.0	-	-	ns	Pins: DB7 - 0

### Read mode



Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
E Cycle Time	$t_c$	400.0	-	-	ns	Pin E
E Pulse Width	$t_{pw}$	150.0	-	-	ns	Pin E
E Rise/Fall Time	$t_r, t_f$	-	-	25.0	ns	Pin E
Address Setup Time	$t_{sp1}$	30.0	-	-	ns	Pins: RS, R/W,E
Address Hold Time	$t_{hp1}$	10.0	-	-	ns	Pins: RS, R/W,E
Data Output Delay Time	$t_d$	-	-	100.0	ns	Pins: DB7 - 0
Data hold time	$t_{hd}$	20.0	-	-	ns	Pin DB7 - 0

## 2.4 Instruction Table

### ◆ Display Control Instruction

Instruction	Instruction Code										Description	Execution time ( $F_{osc} = 270KHz$ )
	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM and set DDRAM address to "00H" from AC	1.52ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.52ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction and enable the shift of entire display	38 $\mu$ s
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	38 $\mu$ s
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display shift control bit, and the direction, without changing of DDRAM data.	38 $\mu$ s
Function Set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-bit/4-bit), numbers of display line (N: 2-line/1-line) and, display font type (F: 5x10 dots/5x8 dots)	38 $\mu$ s
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	38 $\mu$ s
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in counter	38 $\mu$ s
Read Busy Flag and Address Counter	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	38 $\mu$ s
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	38 $\mu$ s

1: don't care



## 2.5 Character Generator ROM

Upper 4 bit Lower 4 bit	1111	1110	1101	1100	1011	1010	1001	1000	0111	0110	0101	0100	0011	0010	0001	0000
1111				Q	W	P	V						一	夕	厶	𠂇
1110			!	1	Q	W	W						𠂇	𠂇	𠂇	𠂇
1101			"	2	B	R	B						𠂇	𠂇	𠂇	𠂇
1100			#	3	C	S	C						𠂇	𠂇	𠂇	𠂇
1011			*	4	D	T	D						𠂇	𠂇	𠂇	𠂇
1010			𠂇	5	E	U	U						𠂇	𠂇	𠂇	𠂇
1001			𠂇	6	F	V	V						𠂇	𠂇	𠂇	𠂇
1000			𠂇	7	G	W	W						𠂇	𠂇	𠂇	𠂇
0111			𠂇	8	H	X	X						𠂇	𠂇	𠂇	𠂇
0110			𠂇	9	I	Y	Y						𠂇	𠂇	𠂇	𠂇
0101			𠂇	*	J	Z	Z						𠂇	𠂇	𠂇	𠂇
0100			𠂇	+	K	L	L						𠂇	𠂇	𠂇	𠂇
0011			𠂇	𠂇	𠂇	𠂇	𠂇						𠂇	𠂇	𠂇	𠂇
0010			𠂇	𠂇	𠂇	𠂇	𠂇						𠂇	𠂇	𠂇	𠂇
0001			𠂇	𠂇	𠂇	𠂇	𠂇						𠂇	𠂇	𠂇	𠂇
0000			𠂇	𠂇	𠂇	𠂇	𠂇						𠂇	𠂇	𠂇	𠂇