

High Power NPN Silicon Power Transistors

... designed for linear amplifiers, series pass regulators, and inductive switching applications.

- Forward Biased Second Breakdown Current Capability
 $I_{S/b} = 3.75 \text{ A}_{dc} @ V_{CE} = 40 \text{ V}_{dc} \text{ — } 2N3771$
 $= 2.5 \text{ A}_{dc} @ V_{CE} = 60 \text{ V}_{dc} \text{ — } 2N3772$

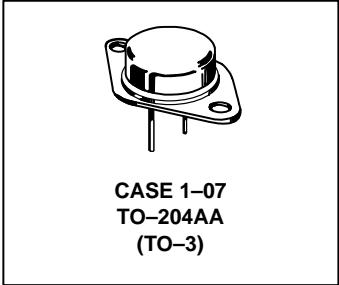
***MAXIMUM RATINGS**

Rating	Symbol	2N3771	2N3772	Unit
Collector–Emitter Voltage	V_{CEO}	40	60	Vdc
Collector–Emitter Voltage	V_{CEX}	50	80	Vdc
Collector–Base Voltage	V_{CB}	50	100	Vdc
Emitter–Base Voltage	V_{EB}	5.0	7.0	Vdc
Collector Current — Continuous Peak	I_C	30 30	20 30	A _{dc}
Base Current — Continuous Peak	I_B	7.5 15	5.0 15	A _{dc}
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	P_D	150 0.855		Watts W/ $^\circ\text{C}$
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200		$^\circ\text{C}$

2N3771 *
2N3772

*ON Semiconductor Preferred Device

**20 and 30 AMPERE
POWER TRANSISTORS
NPN SILICON
40 and 60 VOLTS
150 WATTS**



THERMAL CHARACTERISTICS

Characteristics	Symbol	2N3771, 2N3772	Unit
Thermal Resistance, Junction to Case	θ_{JC}	1.17	$^\circ\text{C}/\text{W}$

*Indicates JEDEC Registered Data.

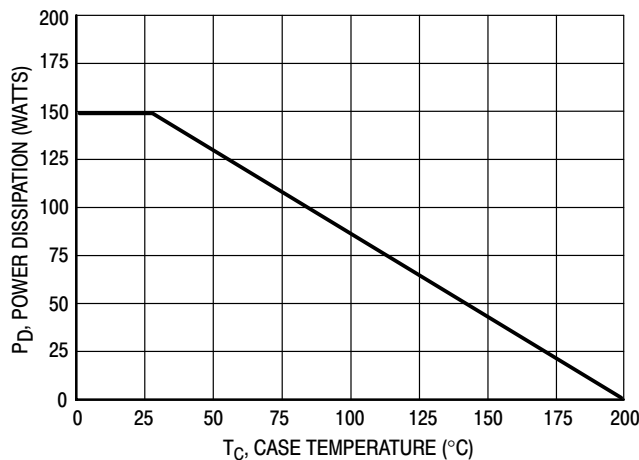


Figure 1. Power Derating

Preferred devices are ON Semiconductor recommended choices for future use and best overall value.

2N3771 2N3772

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
*Collector–Emitter Sustaining Voltage (1) (I _C = 0.2 Adc, I _B = 0)	2N3771 2N3772	V _{CEO(sus)}	40 60	— —	Vdc
Collector–Emitter Sustaining Voltage (I _C = 0.2 Adc, V _{EB(off)} = 1.5 Vdc, R _{BE} = 100 Ohms)	2N3771 2N3772	V _{CEX(sus)}	50 80	— —	Vdc
Collector–Emitter Sustaining Voltage (I _C = 0.2 Adc, R _{BE} = 100 Ohms)	2N3771 2N3772	V _{CER(sus)}	45 70	— —	Vdc
*Collector Cutoff Current (V _{CE} = 30 Vdc, I _B = 0) (V _{CE} = 50 Vdc, I _B = 0) (V _{CE} = 25 Vdc, I _B = 0)	2N3771 2N3772	I _{CEO}	— —	10 10	mAdc
*Collector Cutoff Current (V _{CE} = 50 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 100 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 45 Vdc, V _{EB(off)} = 1.5 Vdc) (V _{CE} = 30 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C) (V _{CE} = 45 Vdc, V _{EB(off)} = 1.5 Vdc, T _C = 150°C)	2N3771 2N3772 2N6257 2N3771 2N3772	I _{CEV}	— — — — —	2.0 5.0 4.0 10 10	mAdc
*Collector Cutoff Current (V _{CB} = 50 Vdc, I _E = 0) (V _{CB} = 100 Vdc, I _E = 0)	2N3771 2N3772	I _{CBO}	— —	2.0 5.0	mAdc
*Emitter Cutoff Current (V _{BE} = 5.0 Vdc, I _C = 0) (V _{BE} = 7.0 Vdc, I _C = 0)	2N3771 2N3772	I _{EBO}	— —	5.0 5.0	mAdc
*ON CHARACTERISTICS					
DC Current Gain (1) (I _C = 15 Adc, V _{CE} = 4.0 Vdc) (I _C = 10 Adc, V _{CE} = 4.0 Vdc) (I _C = 8.0 Adc, V _{CE} = 4.0 Vdc) (I _C = 30 Adc, V _{CE} = 4.0 Vdc) (I _C = 20 Adc, V _{CE} = 4.0 Vdc)	2N3771 2N3772 2N3771 2N3772	h _{FE}	15 15 5.0 5.0	60 60 — —	—
Collector–Emitter Saturation Voltage (I _C = 15 Adc, I _B = 1.5 Adc) (I _C = 10 Adc, I _B = 1.0 Adc) (I _C = 30 Adc, I _B = 6.0 Adc) (I _C = 20 Adc, I _B = 4.0 Adc)	2N3771 2N3772 2N3771 2N3772	V _{CE(sat)}	— — — —	2.0 1.4 4.0 4.0	Vdc
Base–Emitter On Voltage (I _C = 15 Adc, V _{CE} = 4.0 Vdc) (I _C = 10 Adc, V _{CE} = 4.0 Vdc) (I _C = 8.0 Adc, V _{CE} = 4.0 Vdc)	2N3771 2N3772	V _{BE(on)}	— —	2.7 2.2	Vdc
*DYNAMIC CHARACTERISTICS					
Current–Gain — Bandwidth Product (I _C = 1.0 Adc, V _{CE} = 4.0 Vdc, f _{test} = 50 kHz)		f _T	0.2	—	MHz
Small–Signal Current Gain (I _C = 1.0 Adc, V _{CE} = 4.0 Vdc, f = 1.0 kHz)		h _{fe}	40	—	—
SECOND BREAKDOWN					
Second Breakdown Energy with Base Forward Biased, t = 1.0 s (non–repetitive) (V _{CE} = 40 Vdc) (V _{CE} = 60 Vdc)	2N3771 2N3772	I _{S/b}	3.75 2.5	— —	Adc

*Indicates JEDEC Registered Data.

(1) Pulse Test: 300 μs, Rep. Rate 60 cps.

2N3771 2N3772

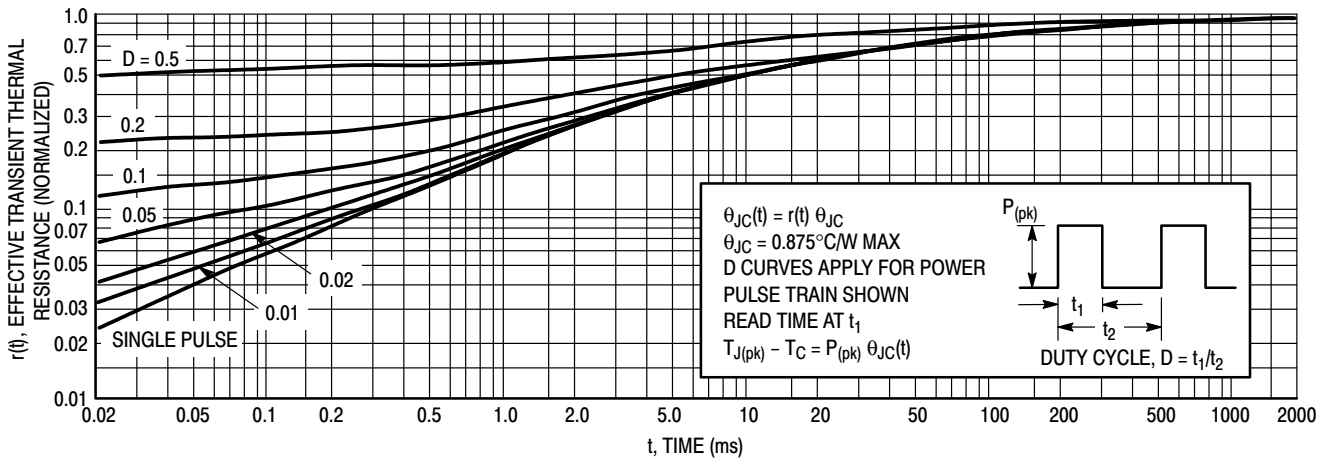


Figure 2. Thermal Response — 2N3771, 2N3772

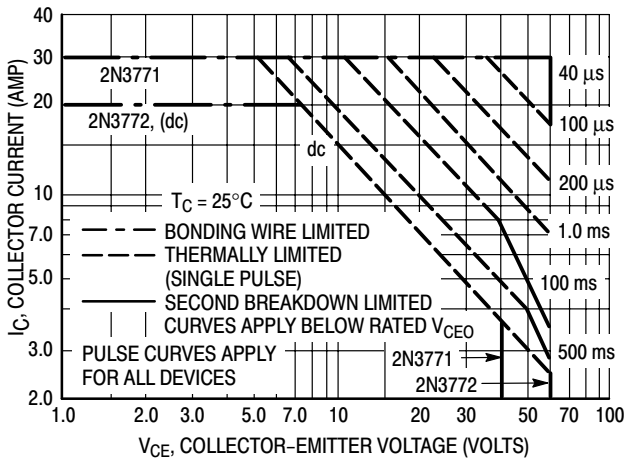


Figure 3. Active-Region Safe Operating Area — 2N3771, 2N3772

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation: i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

Figure 3 is based on JEDEC registered Data. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} < 200^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data of Figure 2. Using data of Figure 2 and the pulse power limits of Figure 3, $T_{J(pk)}$ will be found to be less than $T_{J(max)}$ for pulse widths of 1 ms and less. When using ON Semiconductor transistors, it is permissible to increase the pulse power limits until limited by $T_{J(max)}$.

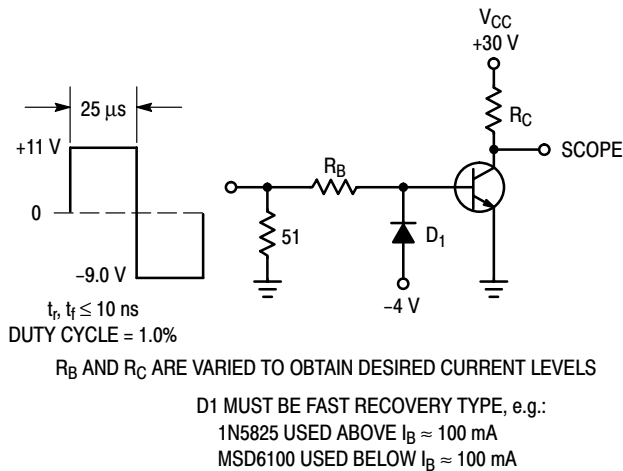


Figure 4. Switching Time Test Circuit

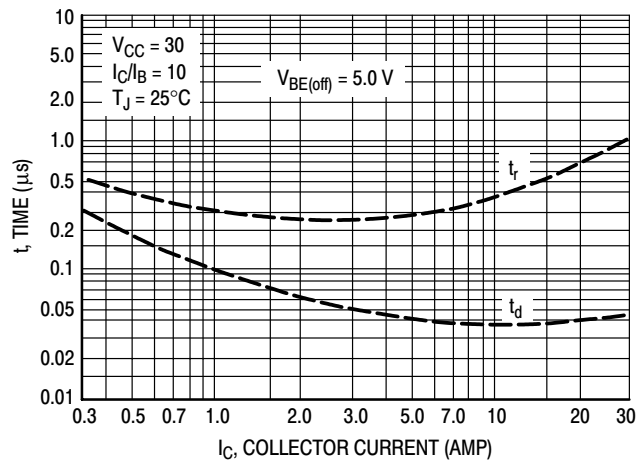


Figure 5. Turn-On Time

2N3771 2N3772

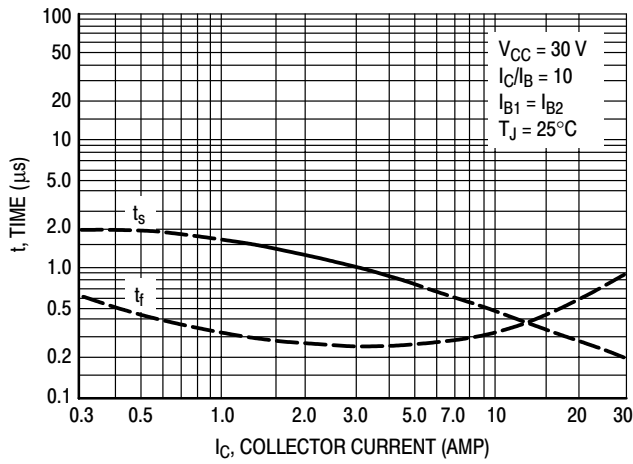


Figure 6. Turn-Off Time

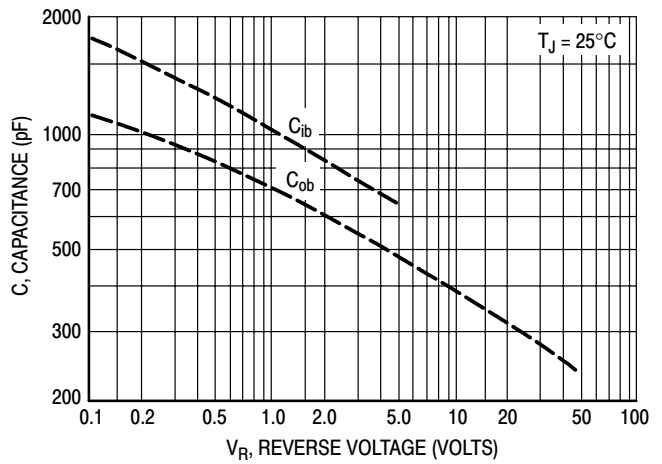


Figure 7. Capacitance

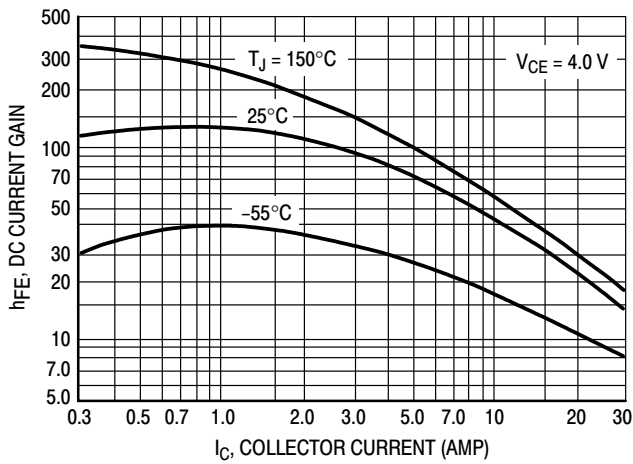


Figure 8. DC Current Gain

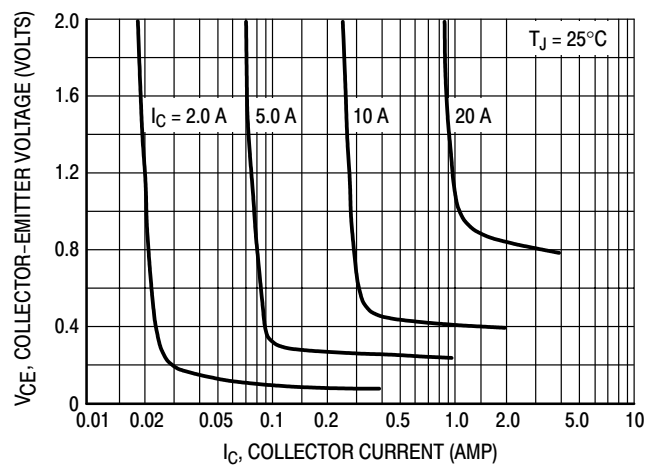
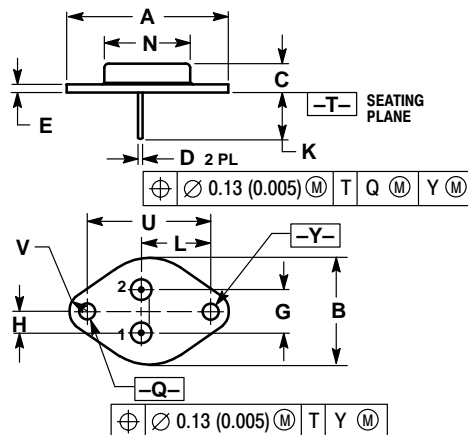


Figure 9. Collector Saturation Region

PACKAGE DIMENSIONS

CASE 1-07 TO-204AA (TO-3) ISSUE Z




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF	---	39.37 REF	---
B	---	1.050	---	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC	---	10.92 BSC	---
H	0.215 BSC	---	5.46 BSC	---
K	0.440	0.480	11.18	12.19
L	0.665 BSC	---	16.89 BSC	---
N	---	0.830	---	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC	---	30.15 BSC	---
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE. COLLECTOR

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